ATM Chips, Product and Vendor List

Christian Paetz*
TU Chemnitz-Zwickau†
Institute of Information Technology‡
Reichenhainer Str.70
D-09126 Chemnitz

October 25, 1994

Abstract

This is the first update of this ATM chip list. A lot of errors were removed and some new chips added. Please continue reporting detected mistakes and ATM chips not listed here. There is a online version of this document available via WWW[1]. This version is always the actual one and contains all the changes as HTML comments.
Christian Paetz[2],(paetz@infotech.tu-chemnitz.de)

1 Switching Fabrics

1.1 Fujitsu MB 86680

The MB 86680 is a 4*4 cell switch building-block, which can be used to construct compact matrices due to its row and column expansion ports. It selects high and low priority queues and it queues the output of a nonblocking internal multiplex bus. It uses a up to 3 Byte long routing tag for both unicast and multicast switching. /3,10/

1.2 Philips PHAME - HSE

4*4 Switching element for data streams up to 622 Mbps, realised in 1,0 μm technology , not available yet

1.3 Ascom Aramis++

Aramis++ is a concept for an ATM switch based on a two-ASIC chip set: the QET (Quad Exchange Termination) and the EASE (Expandable ATM Switching Element). An Aramis++ based ATM switch is scalable between 4x4 and 16x16 I/O ports in steps of 4.

1.4 IBM Prizma

16*16 switching unit, internally switched via flexible shared buffer, current version runs up to 155 Mbps, Line speed of 1 Gbps and above are under development, chip is used in IBM systems only and currently not available for OEM /5/

[1] http://www.infotech.tu-chemnitz.de/www-public/prof-it/dako/atm_chips.html
[2] http://www.infotech.tu-chemnitz.de/www-public/prof-it/dako/mitarbeiter/paetz/paetz.html

1.5 Alcatel ISE Chip

A modular system with line rate up to 155 Mbps, realised in 0,7 ym technology, currently for use in Alcatel devises only

1.6 Mikroelektronik Anwendungszentrum Hamburg MAZ DAS 3xx

MAZ is developing a 4*4 switching matrix for line speeds up to 155 Mbps, not available yet

1.7 AT&T T7650

Switch matrix chip is self routing, scalable design permits use in small and large ATM switch fabrics with data rates up to 300 Mbps. /9/

1.8 Brooktree Bt8215

Bt8215 bidirectional cell buffer supports Brooktree's Bt8220 by enabling full-duplex communication between 32-bit systems or processor busses and 8-bit I/O peripherals. Its enhanced buffering scheme uses three I/O buffer ports rather than the traditional two. Separate 2-Kbyte input and output dual-port memory buffers include all necessary control logic for 8-to-32-bit conversion. Buffers are also provided for dedicated 8-bit input and output ports and a bidirectional 32-bit port. The Bt8215 also includes all control logic necessary to achieve low-cost ATM switching and multiplexing for up to 155-Mbps ports. Low-cost, bus-oriented ATM switches can also be constructed to provide up to 1.2 Gbits/s of total bandwidth. Bt8215 comes in a 100-pin PQFP and costs $ 85 each /1000. /2/

1.9 Supernet Super X - Combined SAR and switch

SuperX is a versatile ASIC device designed with built-in support for a wide range of ATM applications. SuperX combines a SAR controller and switching functionality. The device contains a buffer of 16KByte for up to 292 cells temporary storage. The SuperX principle of operation is based on its ability to switch information units among its three (3) bi-directional ports. The ports and the data format on each one of them are:

- Link port, supports: ATM cells;
- Host port, supports: AAL5 CS_PDU data units and
- X-Bus port, supports: 640 Mbps X-Cells (ATM + routing header)

Incoming cells from each of the inputs can be routed to one or more of the outputs as specified above. Routing of cells inside SuperX is supported by an external Look Up Table (LUT), and internal address filters. The LUT performs ATM label swapping by replacing the cell's incoming header with a new one. The extended header ('X_Header') provides intra SuperX and inter SuperX routing information, and is also read from the LUT. SuperX Features are:

- ATM layer implementation.
- ATM Adaptation Layer 5 (AAL5 - SEAL) implementation.
- On chip 16 KBytes RAM cell buffer (292 cells).
- Built in switching support of link in to link out cell forwarding

- UTOPIA physical interface.
- Adjustable link rate up to 155Mbps.
- High performance processor interface.
- Interface with multiple SuperX devices to create a self contained ATM switch.
- Support for 64K VPI / VCI values.
- VP and VP / VC level switching.
- Support for multiple service priorities.
- Simultaneous segmentation of up to 64 PDUs.
- Simultaneous re-assembly of up to 8192 PDUs.
- Loop back at the ATM and AAL protocol layers.
- Low power CMOS 0.6 μm technology. 208 pins PQFP package.

1.10 Supernet SuperS - Switching fabric

5 Gbps Non blocking switching unit, based on 2 ASIC (SuperY), supports non blocking switching of 8x8 STS-12, 32x32 STS-3, 112x112 STS-1 and any combination of. Dynamic buffer allocation with up to 64K cells buffer per port. Four traffic class controlled by a programmable arbiter.

1.11 TriQuint TQ8016

16 X 16 digital crosspoint switch, 1.3Gbps data rate, non blocking architecture, ECL-level data I/O with fully differential data path, CMOS-level control inputs; 132-pin LCC.

1.12 TriQuint TQ8032

32 X 32 digital crosspoint switch, 800Mbps data rate, otherwise similar to TQ8016.

2 SAR-Controller

2.1 National Semiconductor FRED chip set DP83372 F, DP 83382-R

The Adaptive ATM FRED chips are designed to be used in equipment which interfaces to an ATM network. The functions included are most of the ATM layer, segmentation and reassembly (SAR) and DMA/buffer management functions. The ATM interface chipset is a two-chip set, partitioned into transmit and receive functions, which we refer to as "FRED" (Fragmentation-Reassembly Engine with DMA). This ATM interface chipset is designed to provide network interface functions at a similar level as those provided by a LAN controller:

- On transmit, packet buffers are queued to the FRED, which fragments the packets into standard cells and meters them into the network over virtual circuits at peak and average rates specified a priori by software.

- On receive, cells are accepted from the line, with multiple frames possibly interleaved together, and the cells are verified, headers are stripped, the user data is reassembled into frames, then enqueued for the receiver software when the entire frame has been received.

The chipset can accommodate up to 65K VC's, and up to 8K buffers; external high-speed RAM (such as static RAM) holds state information such as buffer descriptors and VCI's. There can be multiple buffers queued for transmission on any given VC. The transmit side has a flexible transmit rate structure, with up to eight different peak rates, and a leaky bucket-based metering scheme which can have individual parameters for each VC. FRED supports both AAL3/4 and AAL5 concurrently, selectable on a VC-by-VC basis. It also has an AAL bypass mechanism which allows access to "raw cells", again selectable VC-by-VC.

2.2 LSI Logic ATMizer L64360

The ATMizer Architecture provides complete control over ATM Segmentation and Reasembly and all ATM Layer functions. The architecture also includes the ATM Processing Unit, a 32-bit RISC CPU (based on MIPS R3000), which, trough user firmware, controls the functional blocks. Features of the ATMizer architecture are:

- Support ATM rates of up to 155 Mbps
- Simultaneously supports ATM Adaption Layers 1,2,3/4 and 5
- handles continous and non-continous CS-PDUs
- 32 bit DMA addressing capabilities
- supports up to 65536 VCs
- The internal RISC CPU controls:
  - scatter-gather algorithms
  - AAL SAR pDU Header and Trailer translation
  - ATM Header generation and manipulation
  - Error Handling, Congestion Control, statistics,...
- UTOPIA and Standard ATM Interface (SAI)

2.3 Texas Instruments TDC 1560

The TDC 1560 (SAHI) provides complete encapsulation and termination of AAL5, AAL3/4 and has an transparent mode for unsupported AALs. Other features are:

- UTOPIA-Interface
- Glueless Control SRAM, SBUS EPROM and TDC 1500
- SBUS- Interface
- supports 1023 unique VCs
- 32 kbps - 155 Mbps controllable bandwidth range
- 240 pin MQUAD package, price 105 $ each/100 units, not available yet /8/

2.4 TransSwitch TXC 05501/5601

SAR Layer Controller compatible to National Semiconductors FREAD chip set

2.5 NEC μPD98401

Supports AAL Layers 1, 3/4, 5; has UTOPIA Interface

2.6 Fujitsu MB86686

The Adaption Layer Controller provides a complete implementation of both AAL3/4 and AAL5 procedures. User data is transferred to and from system memory via an on-chip high speed DMA controller, which can interface to a variety of 32- and 64-bit bus structures. The MB 86686 is a full bidirectional device and can support up to 1K simultaneous connections in both receive and transmit directions and network speed up to 155 Mbps. Other features are

- leaky bucket averaging algorithm for each VC
- programmable peak and average rate for total cell stream output
- routing tag generation for Fujitzu MB 86680 switching element /3/

3 Physical Layer Controller

3.1 Brooktree BT 8210/8220/8230

Brooktree's Bt8220 ATM transmitter/receiver chip supports data rates from 34 Mbits/s to 155 Mbits/s when used with two line interface units (LIUs); the electrical interfaces can be supported with one external LIU and the optical interfaces with a second LIU. Bt8220 provides industry-standard physical layer convergence procedure (PLCP) for DS1, E1, DS3, E3, and cell alignment via header check sequence (HCS). It also generates and checks all overhead for ATM Adaption Layer (AAL) 1, 3/4 and 5 formatted payloads. And its array of seven integrated framers provides for programmable interfaces. The list of framers includes a G.804 framer for European ATM standards, plus framers for DS3/E3, STS-1, E4, STS-3c and STM-1 data streams. External framer ICs, also made by Brooktree, can be connected directly to the Bt8220 for data rates not internally framed. Bt8220 is a 160-pin PQFP that costs $90 each/1000./2/

3.2 TransSwitch TXC-05150

cell delineation block (CDB) supports framing of DS-1/3, E-1/2/3, STS-1/3C and STM 1

3.3 Texas Instruments TDC 1500 (SABRE)

This is a single chip physical layer controller for 155 Mbps. It includes

- full duplex (Tx/Rx) operation
- on chip clock recovery and clock generation using analog PLL
- SONET framing
- Limited overhead termination (following ATM Forum)

- UTOPIA cell interface
- three cell input and output FIFO buffers

The chip comes as 144 pin PQFP for 105 $ (100 units)

3.4 Texas Instruments TDC 2301 B / TDC 2302 B

SONET/SDH Frame Synchronizer , 84 pin PLCC, Price 60 $ each/100 units

3.5 Texas Instruments TDC 3003

STS3 Overhead Terminator, 160 pin PQFP, Price 190 $ each/100 units.

3.6 TriQuint GA 9101 / 9102

Transmitter and / receiver pair, ATM- and ESCON-compatible. TTL-compatible 10-bit-wide data bus with 19.44MHz, 20.00MHz, or 26.5625MHz byte clock; serial rates of 194.4Mbps, 200.0Mbps, or 265.625Mbps; PLL clock generation and recovery; expect 8B/10B data encoding.

3.7 PMC Sierra PM 5345

The PM5345 SUNI chip maps ATM cells from an ATM switch core or an adaptation layer processor into the SONET payload, adds SONET-based framing and overhead according to ANSI and CCITT recommendations and the ATM Forum UNI specification. The device contains on-chip serial-to-parallel conversion operating at 155 MHz, and utilizes pseudo-ECL inputs and outputs for the high speed signals. This allows the SUNI to directly interface with commercially available optical modules and clock recovery circuits and to twisted pair interface circuits for operation over category-5 unshielded twisted pair wiring (UTP-5). The system side interface of the SUNI can operate in either 8-bit or 16-bit mode, up to 25 MHz. On chip overhead expansion logic allows access to all of the SONET overhead bytes so that external logic can expand the function to a full Network-Node Interface (NNI) compliant SONET-ATM function for use in public network applications. The device is packaged in a 160 pin plastic quad flat pack (PQFP). The SUNI PM 5345 $68.00 in 10K quantities. /11/

3.8 PMC Sierra PM5346 - S/UNI-Lite

The S/UNI-Lite is a LAN optimized second generation of the PM5345 S/UNI product (aka the S/UNI Classic). The delta from the S/UNI includes the addition of integrated clock and data recovery (fully compliant to SONET/SDH jitter specifications) on-chip, support for 51 Mb/s, a synchronous 8 bit SCI-PHY system interface (SCI-PHY is PMC's Saturn Compliant Interface for the PHYsical layer - a superset of the Utopia interface), and link level GFC support. The part is packaged in a 14 by 20mm 128 Pin PQFP.

3.9 PMC Sierra PM5347 - S/UNI-PLUS

The S/UNI-PLUS is a WAN optimized second generation of the PM5345 S/UNI product. The delta from the S/UNI includes the addition of integrated clock and data recovery (fully compliant to SONET/SDH jitter specifications) on-chip, support for 51 Mb/s, a synchronous 8/16 bit SCI-PHY system interface, individual serialized interface to all overhead functions, integrated protection switching support (K1, K2), section and path trace, and link level GFC support. The part is packaged in a 208 Pin PQFP.

3.10 PMC Sierra PM 7345

SATURN-UNI, User Network Interface chip DS-3 and E-3 PDH (34 Mbps / 45 Mbps)

3.11 PMC Sierra PM 5712/14, PM 5318, PM 5345

The PM5712 serves as a 622-Mbit/s interface between optical fibers and four 155-Mbit/s data streams. PM5712 is a 182-pin Kovar flat pack that costs $1100 in OEM quantities. Two of the ICs used in the module can be purchased separately; they are the PM5318 serial-to-parallel conversion chip (128-pin PQFP; $120 each/10,000) and the PM5312 SONET/SDH transport terminating transceiver (208-pin PQFP; $170 each/10,000).

3.12 PMC Sierra PM 5355

The S/UNI-622 provides SONET/SDH framing and overhead processing and ATM cell processing for 622 Mb/s STM-4/STS-12c interfaces. Details will be announced later.

3.13 PMC Sierra PM 7321

Implements the Physical Layer Convergence Protocol for DS1 an DS3 based PLCP according to TA-TSY-000773 and TA-TSY-000772 and IEEE Std 802.6-1990, Implements the Physical Layer Convergence Protocol for E1 and E3 based PLCP according to the ETSI Draft Standards T/NA(91)17, and T/NA(91)18, Provides on-chip 4-cell FIFO buffers in both transmit and receive paths, supports arbitrary rate external transmission system interface up to a maximum rate of 52 Mbit/s, provides an integral framer to support M23 or C-bit parity DS3 formats with path maintenance data link processing and bit-oriented code support for FEAC channel termination, 84 pin PLCC package price (in OEM Quantity) 80 US-$

3.14 PMC Sierra PM7345

The S/UNI-PDH is a second generation enhancement to the PM7321 PLPP. In addition to all of the functionality previously provided by the PM7321 - the S/UNI-PDH provides an integrated E3 framer (both G.751 and G.832), supports E3 trail trace. The part is packaged in an 84 Pin PLCC (Backwards compatible with the PM7321) and also in a 14 by 14mm 100 Pin PQFP. Note that both the PLPP and S/UNI-PDH chips interface seamlessly with the PM4341A and PM6341 T1/E1 single chip framer/LIU chips for use in T1/E1 ATM UNI's.

3.15 Raytheon RCC 700

A pair of transmitter/receiver ICs from Raytheon, namely the RCC700 and RCC701, support ATM systems at rates up to 194.4 Mbaud and interface directly to fiber optic transceivers. RCC700 integrates an 8-bit/10-bit (8b/10b) encoder/decoder, a serializer, a de-serializer, a PLL frequency synthesizer, a PLL clock, and data recovery and byte alignment circuitry. RCC700's transmitter section accepts a TLL/CMOS compatible parallel byte from a controller IC, encodes the data using

8b/10b code, synthesizes the high-speed clock, and serializes the data into a differential PECL (positive-shifted ECL, Vth=+3.7V) compatible output. The receiver section performs the reverse operations, as well as clock and data recovery, byte alignment, and error detection functions. Where the 8b/10b encoder and decoder functions are not required, Raytheon offers the RCC701, which instead provides a 10-bit parallel interface. In OEM quantities, RCC700 costs $32.10 in 68-pin PLCCs and $33.30 in 64-pin PQFPs; RCC701 costs $29.90 in 68-pin PLCCs and $30.90 in 64-pin PQFPs.

3.16 Raytheon RCC 521

The TCC 521 STS/3 Synchronizer and Framer provides all the frame recognition and synchronisation functions required of a SONET/SDH line interface. It performs

- on-chip clock recovery and clock synthesis
- PECL I/O for direct interface to fiber-optic modules
- Receives 19.44 Mhz byte clock and byte data from terminal and provides serial data to network
- Scrambling/descrambling and BIP 8 calculation/checking with optional bypass mode

3.17 AMCC S 3011/ 3012, S 3005 / 3006

S3005/S3006 transmitter/receiver chipset provide an 8-bit TTL/CMOS-compatible interface and comes in 68-pin leaded chip carrier packages (LDCCs). They are available in speed options of 155.52 Mbit/s ($49 each/1000) and 622.08 Mbit/s ($99 each/1000). S3014 Clock synthesis/recovery IC is supplied in a 44-pin PLCC; in synthesis mode it generates either a 155.52-Mbit/s stream ($41 each/1000) of a 622.08-Mbit/s stream ($65 each/1000); in receive mode it accepts a scrambled NRZ signal, recovers the clock, and retimes the data. S 3011/ 3012 are for STP / UTP while S 3005 / 3006 are for optical link connection.

3.18 Fujitsu MB 86683

Implements all TC sublayer functions for physical media based on SONET/SDH, DS3, E3 and unframed cells, support for framed physical layer OAM functions, direct connection to external transceiver via 8 bit parallel interface, generates 3 Byte routing tag for Fujitsu MB 86680 switching matrix, interfaces directly to address translation controller to perform realtime cell header translation, supplied in 176 pin PQFP./10/

3.19 NEC μPD 98402

SONET STS 3 (155 Mbps) framer with DMA host interface, UTOPIA-Interface

3.20 Integrated Telecom Technology WAC-034-A / WAC-013-A

Framer & formatter for DS 3, E 3 and E 4 formats, SONET frames, up to 155 Mbps data rate

4 Transceiver

4.1 National Semiconductor DP83223

This Twisted Pair Transceiver is an integrated circuit capable of driving and receiving either two-level (binary) encoded or three-level (MLT-3) encoded datastreams. The DP83223 allows links of up to 100 meters over both STP and UTP. It is provided in 28 pin PLCC.

4.2 Micro Linear ML6672 + ML 6633/6622

The ML 6672 is a complete monolithic transceiver for 155 Mbaud NRZ encoded data transmissionover Category 5 Unshielded Twisted Pair and Shielded Twisted Pair cables. The adaptiveequalizer in the ML 6672 will accurately compensate for line losses of up to 100m UTP. The ML6672 receive section consists of an equalizing filter with feedback loop for controlling effective line compensation. ML 6633/6622 are for fiber./7/

4.3 Texas Instruments TDC 1555/TDC 1556

The TDC 1555 receives an embedded clock signal from a 155 Mbps STS3 NRZ data stream using a frequency/phase lock loop. It is available in 24 pin DIL package, price (100 units) 50 $.

4.4 Texas Instruments TDC 1522

622 Mb/s Clock recovery chip, not available yet

4.5 AMCC 3014 PLL

The function of the S3014 clock synthesis and recovery unit is to derive high speed timing signals for SONET/SDH based equipment. In clock recovery mode, the S3014 receives either an STS-3/STM1 or STS12/STM4 scrambled NRZ signal and recovers the clock from the data. In clock synthesis mode, the S3014 receives a 19.44, 51,84 or 155.52 Mhz reference clock and outputs an STS3/STM1 or STS12/STM4 differential ECL clock.

4.6 AMD TAXI Am 7968 / Am 7969

TAXI transceiver Bipolar chip set encodes/decodes 4B5B and performs clock recovery. Capable of speeds from 40-175 Mbps

4.7 Cypress CY 7B951 SST

Transceiver supports OC1 (51 Mbps) and OPC-3 (155 Mbps) data streams /6/

5 Line Driver and Magnetics Modules

5.1 Sumitomo Electric ES-9304-T / ES-9216-R

Transmitter and receiver both operate at 1300 nm, with the transmitter typically coupling -10dBm into a single-mode fiber, whereas the sensitivity of the receiver is typically -33 dBm. Both modules combined dissipate 1W from a 5V supply. Signal detect and recovered clock output are provided with the receiver. The modules are molded in plastic, measure 36.4 mm x 15.2 mm x 8.9 mm, and have a 2 x 12 pinout.

Termination is via either FC or SC single mode pigtail. The Tx/Rx pair costs $1300 each in small quantities.

5.2 Hewlett Packard HFBR 5203 / 5204 / 5205

The 5205 is a 1300 nm product with optical performance compilant with the SONET STS-3 Physical Layer specification. The 5204 is similar to the 5205 except the lower cost SONET link for distances up to 500 m (5205 has 2 km range). The HFBR 5203 is the 800 nm alternative for SONERT links up to 150 m. All transceivers are supplied in the new standard 1x9 SIP package style with a duplex SC connector interface for 62.5/125μm multimode fiber optic cables. Are prices are from 120 (5203)to200 (5205) for single pieces.

5.3 Bel FUSE 0556-3899-04 and -05

This interface module can provide the required isolation between the transceiver IC and the physical medium. This module can be employed virtually, with any high speed communication in the twisted pair medium like ATM or FDDI.

5.4 Pulse PE 65620M

For isolation between transceiver chip and physical medium. Designed for use with National Semiconductor DP 83223 "Twister" Chip, Provied in SMD.

5.5 Valor ST 6021/23/25

This 155 Mbps transformer ST 6021 provided a complete magnetics interface for ATM over Category 5 UTP cable. The ST 6025 is similar to the ST 6021 model but additionally provides termination of unused Twisted Pair via a centertapped auto transformer on the cable output in accordance with implementation guidelines. The ST 6021 and ST6023 provide transformer solution for 155 Mbps ATM applications. The ST 6023 performs 200 ohms to 100 ohms impedance matching for the receive channel while the ST6021 provides isolation for the transmit channel. SIL or low profile surface mount package available.

6 Vendor adresses

- Alcatel SEL AG

  Lorenzstr. 10, D-70430 Stuttgart, Phone +49 711 869 6817

- AMD

  Sunnyvale, CA, Phone: (617) 329 4700

- Applied Micro Circuits Coproration

  6195 Lusk Boulevard, San Diego CA 92121, Phone: (619) 450 9333, FAX: (619) 450 9885

- Ascom Tech, Broadband Technology

  Berne Technopark, Morgenstrasse, 129, CH-30118 Berne, Switzerland, Phone 031/999 13 76, Fax 031/999 36 07 Email: office@tech.ascom.ch

- AT&T

  Allentown, PA, Phone: (800) 372 2447

- bel FUSE

  198 Van Vorst Streer, Jersey City, NY, 07302, Phone: (201) 432 0463, Fax: (201) 432 9542

- Brooktree Corporation

  9868 Scranton Road, San Diego CA 92121, Phone: (619)452 7580, Fax: (619)452 1249

- Cypress Semiconductor

  San Diego, CA Phone: (619) 452 7580

- Fujitsu Microelectronics Inc.

  3545 Morth First Street, San Jose CA 95134, Phone: (408) 922 9000, Fax: (408) 431 9044

- Hewlett Packard

  Hewlett-Packard-Str., D-61352 Bad Homburg, Phone: (+49) 6172 15 - 16 34, Fax: (+49) 6172 16 67

- IBM ENC GmbH

  Vangerowstr. 18, D-69115 Heidelberg, Phone: +49 6221 593 000

- Integrated Telecom Technology (IgT)

  18310 Montgomery Village Avenue, Suite 300, Gathersburg MD, 20879, Phone: (301) 990 9890, Fax: (301) 990 9893

- LSI Logic Corperation

  1551 McCarthy Boulevard, Milpitas, CA, 95035, Phone: 408 433 2801,Fax: 408 433 1561, Email (Mr. Michael Barar, Technical Manager): barar@lsil.com

- Microelektronik Anwenderzentrum Hamburg

  Karnapp 20, D-21079 Hamburg, Germany, Phone +49 40 76629 1623, Fax: +41 40 76629 199

- Micro Linear

  2092 Concource Drive, San Jose, CA, 95131, Phone: (408) 721-5200

- National Semiconductor

  2900 Semiconductor Drive, P.O. Box 58090, Santa Clara, CA, 95052, Phone: (408) 721 5000

- NEC

  Mountain View, CA, Phone: (800) 366 9782

- Philips Network System

  Thurn-und-Taxis-Str. 10, D-90411 Nuernberg, Phone: +49 911 526 5144, Fax: +49 911 526 4102

- PMC Sierra Inc.

  8501 Commerce Court, Burnaby, BC, Canada, V5A 4N3, Phone: (604), 668 7300, Fax: (604) 668 7301

- Pulse Engeneering Inc.

  P.O.Box. 12235, San Diego, CA, 92112, Phone: (619) 674 8100

- Raytheon Semiconductor

  350 Ellis Street, Montain View CA 94043, Phone: (800) 722 7074, Fax.: (415)966 7742

- Sumotomo Electric Fiber Optics Corp.

  777 Old Saw Mill River Rd., Suite 230, Tarrytown, NY 10591-6725, Phone: (914) 347 3770, Fax: (914) 347 3863

- SuperNet networking

  576 5th Ave Suite 1103, New York, NY 10036. Phone (212) 221-5998, Fax (212) 724-2220, Email: marketing@supernet.com

- Texas Instruments

  Dallas, TX, Phone: (214) 995 2011

- TransSwitch Corporation

  8 Progress Drive, Shelton, CT, 06484, Phone: (203) 929 8810, Fax: (203) 926 9453

- TriQuint Semiconductor

  2300 Owen Street, Santa Clara, California 95054 USA, Phone: 408-982-0900, Fax: 408-982-0222

- Valor Electronics Inc.

  9715 Business Park Avenue, San Diego, CA, 92131, Phone: (619) 537 2500, Fax: 619 537 2525

References

[1] Goldberg, Lee: ATM Silicon: Ready for Takeoff, Electronic Design, April, 4th 1994, p.51-65

[2] Product Advertisement, EE Product News, Jan. 1994

[3] Fujitsu brochure Asynchronous Transfer Mode, ICs for ATM 1993

[4] USENET comp.dcom.cell-relay, frequently asked questions and newsgroup adds

[5] W.E. Denzel, P.J. Engpersen, I. Iliadis: A Flexible Shared-Buffer, Switch for ATM at Gb/s Rates, Computer Networks & ISDN Systems, 1993

[6] Warren, Andrews: Chips attack ATM physical layer, Computer Design, v33, April 1994

[7] Child, Jeff: Chip enables ATM over copper wire (Mirco Linear‘s ML6672 transceiver),Computer Design, v33, March 1994

[8] McLeod, Jonah: TI, Sun chips halve ATM adapter cost, Electronics, v67, January 1994

[9] Quinnell, Richard A.: Smart ATM switch self-routes cells (modell T7650 from AT&T), EDN v39, March 1994

[10] :Fujitzu give ATM the "set of chips" treatement, Electronic Engineering, v65 November 1993

[11] Leonhard, Milt: Interface chip brings ATM LANs to the desktop (PM5345 SUNI from PMC-Sierra Inc.) Electronic Design v41, June 1993