commodore semiconductor group

NMOS

MPS

6530

MEMORY, I/O, TIMER ARRAY

6530 (MEMORY, I/O, TIMER ARRAY)

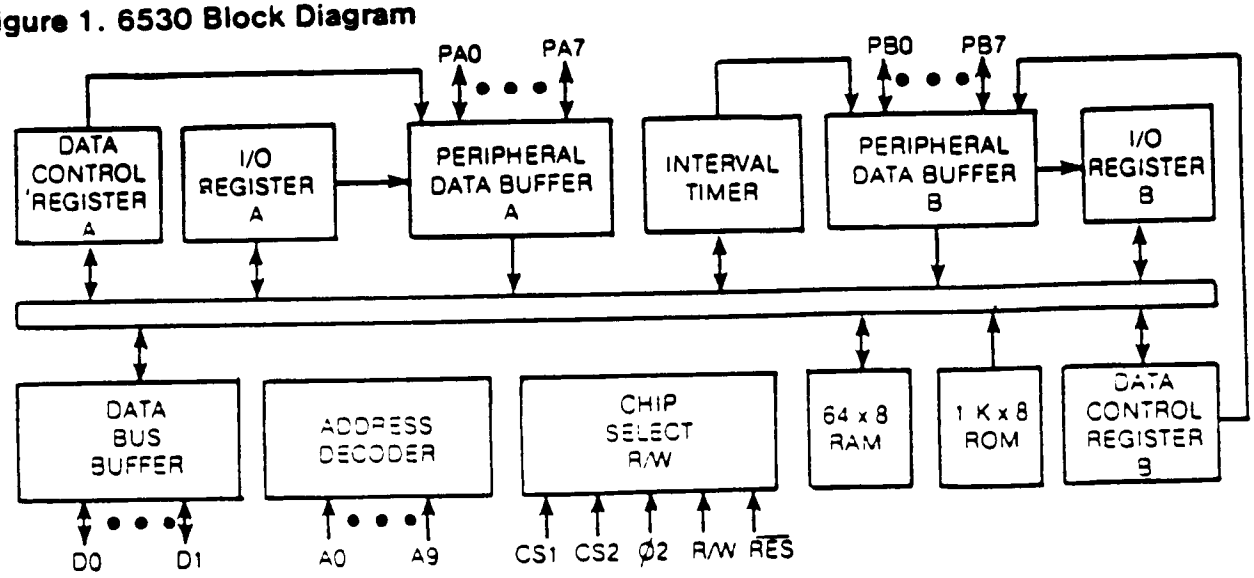
DESCRIPTION

The 6530 is designed to operate in conjunction with the 650X Microprocessor Family. It is comprised of a mask programmable 1024 x 8 ROM, a 64 x 8 static RAM, two software controlled 8 bit bi-directional data ports allowing direct interfacing between the microprocessor unit and peripheral devices, and a software programmable interval timer with interrupt, capable of timing in various intervals from 1 to 262,144 clock periods.

FEATURES

- 8 bit bi-directional Data Bus for direct communication with the microprocessor
- 1024 x 8 ROM
- 64 x 8 static RAM
- Two 8 bit bi-directional data ports for interface to peripherals
- Two programmable I/O Peripheral Data Direction Registers
- Programmable Interval Timer
- Programmable Interval Timer Interrupt
- TTL & CMOS compatible peripheral lines
- Peripheral pins with Direct Transistor Drive Capability
- High Impedance Three-State Data Pins
- Allows up to 7K contiguous bytes of ROM with no external decoding

Figure 1. 6530 Block Diagram



MAXIMUM RATINGS

Supply Voltage, V_{CC}	−0.3V to +7.0V
Input/Output Voltage, V_{IN}	−0.3V to +7.0V
Operating Temperature, T_{OP}	0 C to 70 C
Storage Temperature, T_{STG}	−55 C to 150 C

All inputs contain protection circuitry to prevent damage due to high static discharges. Care should be exercised to prevent unnecessary application of voltages in excess of the allowable limits.

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC}=5.0v±5%, V_{SS}=0v, T_A=25° C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage	V_{IH}	V_{SS}+2.4		V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}−.3		V_{SS}+.4	V
Input Leakage Current: V_{IN}=V_{SS}+5v A0-A9, RS, R/W, $\overline{RES}$, Ø2, PB6*, PB5*	I_{IN}		1.0	2.5	µA
Input Leakage Current for High Impedance State (Three State): V_{IN}=.4v to 2.4v; D0-D7	I_{TSI}		±1.0	±10.0	µA
Input High Current; V_{IN}=2.4v PA0-PA7, PB0-PB7	I_{IH}	−100.	−300.		µA
Input Low Current; V_{IN}=.4v PA0-PA7, PB0-PB7	I_{IL}		−1.0	−1.6	MA
Output High Voltage V_{CC}=MIN, I_{LOAD} ≤ −100µA(PA0-PA7,PB0-PB7,D0-D7) I_{LOAD} ≤ −3 MA (PA0-PB0)	V_{OH}	V_{SS}+2.4 V_{SS}+1.5			V
Output Low Voltage V_{CC}=MIN, I_{LOAD} ≤ 1.6MA	V_{OL}			V_{SS}+.4	V
Output High Current (Sourcing); V_{OH} ≥ 2.4v (PA0-PA7,PB0-PB7,D0-D7) ≥ 1.5v Available for other than TTL (Darlingtons) (PA0,PB0)	I_{OH}	−100 −3.0	−1000 −5.0		uA MA
Output Low Current (Sinking); VOL ≤ .4v (PA0-PA7) (PB0-PB7)	I_{OL}	1.6			MA
Clock Input Capacitance	C_{Clk}			30	pF
Input Capacitance	C_{IN}			10	pF
Output Capacitance	C_{OUT}			10	pF
Power Dissipation	P_D		500	1000	MW

*When programmed as address pins. All values are D.C. readings.

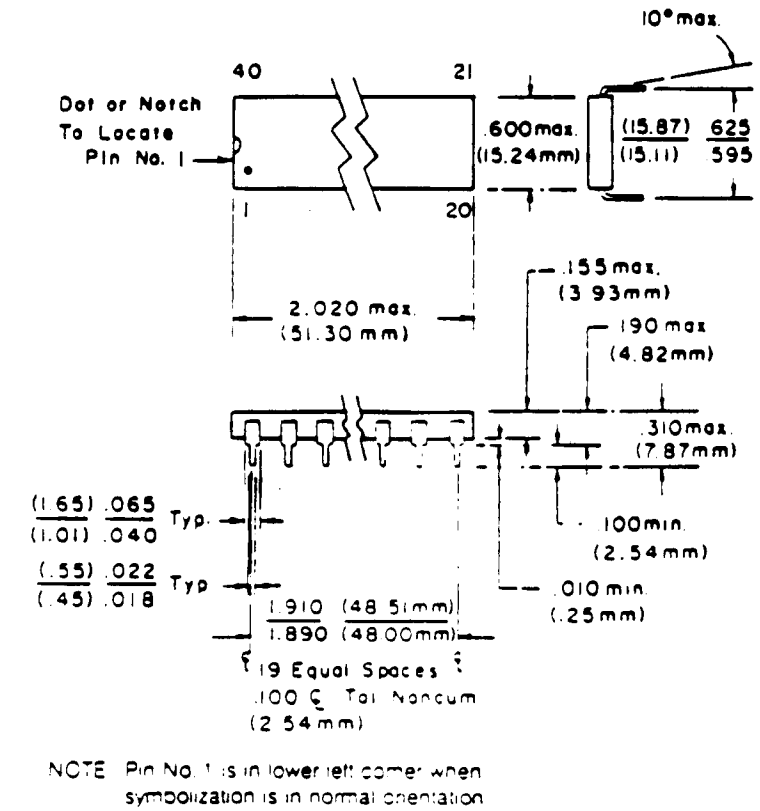
ADDRESSING DECODE

	ROM SELECT	RAM SELECT	I/O TIMER SELECT	R/W	A3	A2	A1	A0
READ ROM	1	*0	0	1	X	X	X	X
WRITE RAM	0	1	0	0	X	X	X	X
READ RAM	0	1	0	1	X	X	X	X
WRITE DDRA	0	0	1	0	X	0	0	1
READ DDRA	0	0	1	1	X	0	0	1
WRITE DDRB	0	0	1	0	X	0	1	1
READ DDRB	0	0	1	1	X	0	1	1
WRITE PER. REG. A	0	0	1	0	X	0	0	0
READ PER. REG. A	0	0	1	1	X	0	0	0
WRITE PER. REG. B	0	0	1	0	X	0	1	0
READ PER. REG. B	0	0	1	1	X	0	1	0
WRITE TIMER								
÷ 1T	0	0	1	0	*	1	0	0
÷ 8T	0	0	1	0	*	1	0	1
÷ 64T	0	0	1	0	*	1	1	0
÷ 1024T	0	0	1	0	*	1	1	1
READ TIMER	0	0	1	1	*	1	X	0
READ INTERRUPT FLAG	0	0	1	1	X	1	X	1

*A_3 = 1 Enables IRQ to PB7

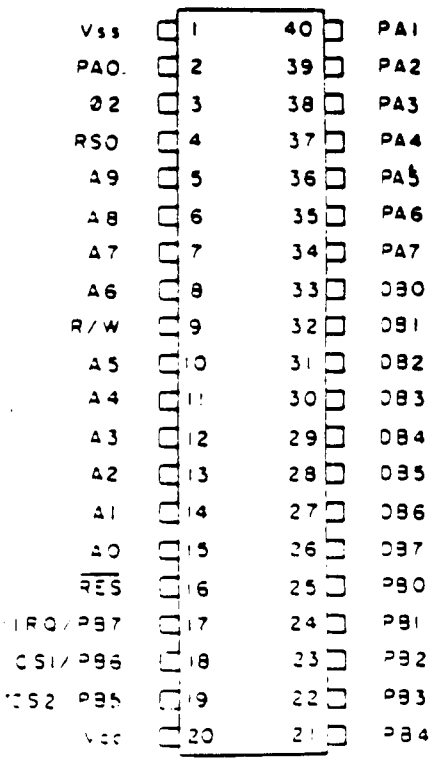
A_3 = 0 Disables IRQ to PB7

Figure 8. Addressing Decode for I/O Register and Timer



NOTE Pin No. 1 is in lower left corner when symbolization is in normal orientation

PACKAGE OUTLINE



6530 PIN DESIGNATION

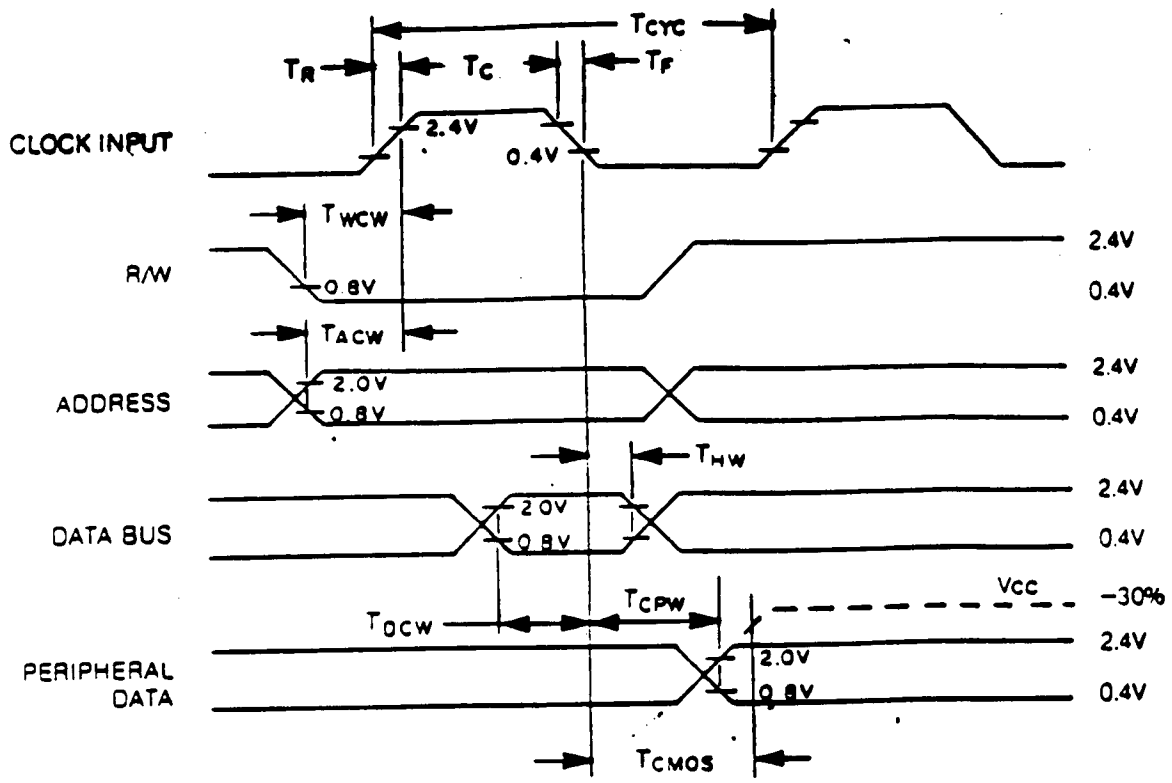


Figure 2 Write Timing Characteristics

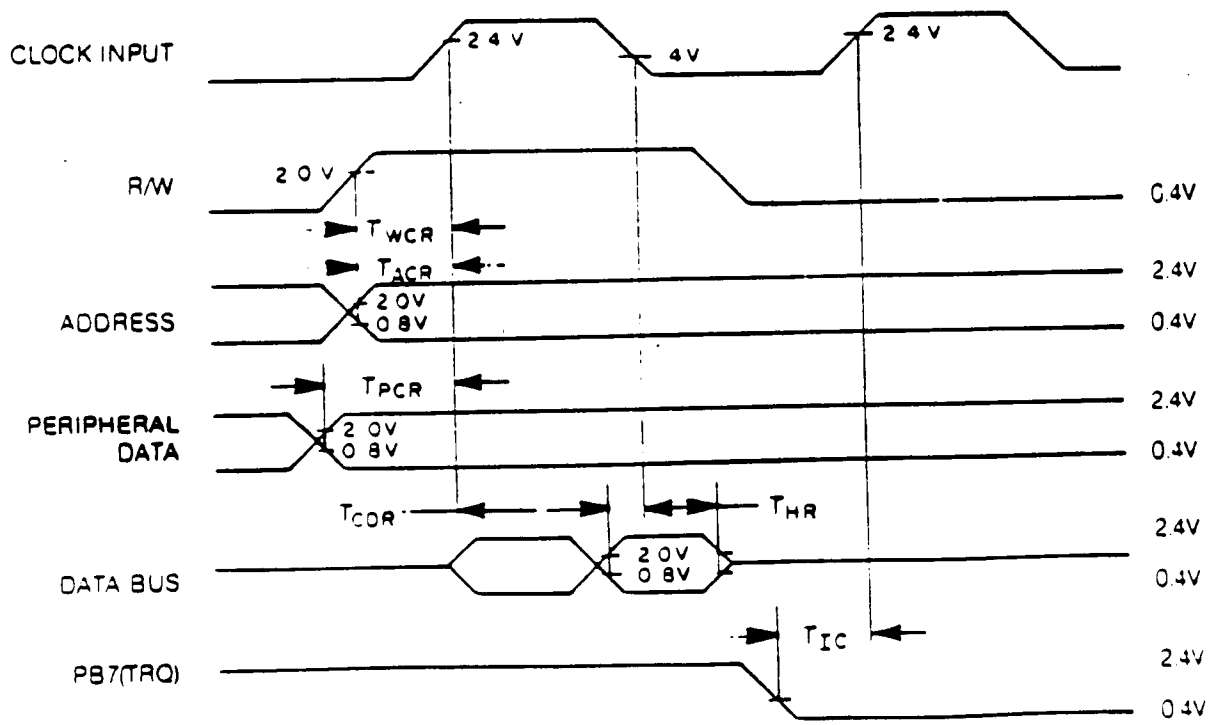


Figure 3 Read Timing Characteristics

WRITE TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Clock Period	TCYC	1		10	μS
Rise & Fall Times	TR, TF			25	NS
Clock Pulse Width	TC	470			NS
R/W valid before positive transition of clock	TWCW	180			NS
Address valid before positive transition of clock	TACW	180			NS
Data Bus valid before negative transition of clock	TDCW	300			NS
Data Bus Hold Time	THW	10			NS
Peripheral data valid after negative transition of clock	TCPW			1	μS
Peripheral data valid after negative transition of clock driving CMOS (Level=VCC−30%)	TCMOS			2	μS

READ TIMING CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
R/W valid before positive transition of clock	TWCR	180			NS
Address valid before positive transition of clock	TACR	180			NS
Peripheral data valid before positive transition of clock	TPCR	300			NS
Data Bus valid after positive transition of clock	TCDR			395	NS
Data Bus Hold Time	THR	10			NS
$\overline{IRQ}$ (Interval Timer Interrupt) valid before positive transition of clock	TIC	200			NS

Loading= 30 pF + 1 TTL load for PA0-PA7, PB0-PB7
=130 pF + 1 TTL load for D0-D7

INTERNAL ORGANIZATION

A block diagram of the internal architecture is shown in Figure 1. The 6530 is divided into four basic sections, RAM, ROM, I/O and TIMER. The RAM and ROM interface directly with the microprocessor through the system data bus and address lines. The I/O section consists of 2 8-bit halves. Each half contains a Data Direction Register (DDR) and an I/O Register.

ROM 1K Byte (8K Bits)

The 8K ROM is in a 1024 x 8 configuration. Address lines A0-A9, as well as RS0 are needed to address the entire ROM. With the addition of CS1 and CS2, seven 6530's may be addressed, giving 7168 x 8 bits of contiguous ROM.

RAM — 64 Bytes (512 Bits)

A 64 x 8 static RAM is contained on the 6530. It is addressed by A0-A5 (Byte Select), RS0, A6, A7, A8, A9 and, depending on the number of chips in the system, CS1 and CS2.

Internal Peripheral Registers

There are four internal registers, two data direction registers and two peripheral I/O data registers. The two data direction registers (A side and B side) control the direction of the data into and out of the peripheral pins. A "1" written into the Data Direction Register sets up the corresponding peripheral buffer pin as an output. Therefore, anything then written into the I/O Register will appear on that corresponding peripheral pin. A "0" written into the DDR inhibits the output buffer from transmitting data to or from the I/O Register. For example, a "1" loaded into data direction register A, position 3, sets up peripheral pin PA3 as an output. If a "0" had been loaded, PA3 would be configured as an input and remain in the high state. The two data I/O registers are used to latch data from the Data Bus during a Write operation until the peripheral device can read the data supplied by the microprocessor array.

During a read operation the microprocessor is not reading the I/O Registers but in fact is reading the peripheral data pins. For the peripheral data pins which are programmed as outputs the microprocessor will read the corresponding data bits of the I/O Register. The only way the I/O Register data can be changed is by a microprocessor Write operation. The I/O Register is not affected by a Read of the data on the peripheral pins.

Interval Timer

The Timer section of the 6530 contains three basic parts: preliminary divide down register, programmable 8-bit register and interrupt logic. These are illustrated in Figure 4.

The interval timer can be programmed to count up to 256 time intervals. Each time interval can be either 1T, 8T, 64T or 1024T increments, where T is the system clock period. When a full count is reached, an interrupt flag is set to a logic "1." After the interrupt flag is set the internal clock begins counting down to a maximum of −255T. Thus, after the interrupt flag is set, a Read of the timer will tell how long since the flag was set up to a maximum of 255T.

The 8 bit system Data Bus is used to transfer data to and from the Interval Timer. If a count of 52 time intervals were to be counted, the pattern 0 0 1 1 0 1 0 0 would be put on the Data Bus and written into the Interval Time register.

At the same time that data is being written to the Interval Timer, the counting intervals of 1, 8, 64, 1024T are decoded from address lines A0 and A1. During a Read or Write operation address line A3 controls the interrupt capability of PB7, i.e., $A_3 = 1$ enables IRQ on PB7, $A_3 = 0$ disables IRQ on PB7. When PB7 is to be used as an interrupt flag with the interval timer it should be programmed as an input. If PB7 is enabled by A3 and an interrupt occurs PB7 will go low. When the timer is read prior to the interrupt flag being set, the number of time intervals remaining will be read, i.e., 51, 50, 49, etc.

INTERFACE SIGNAL DESCRIPTION

Reset ($\overline{RES}$)

During system initialization a Logic "0" on the $\overline{RES}$ input will cause a zeroing of all four I/O registers. This in turn will cause all I/O buses to act as inputs thus protecting external components from possible damage and erroneous data while the system is being configured under software control. The Data Bus Buffers are put into an OFF-STATE during Reset. Interrupt capability is disabled with the $\overline{RES}$ signal. The $\overline{RES}$ signal must be held low for at least one clock period when reset is required.

Input Clock

The input clock is a system Phase Two clock which can be either a low level clock ($V_{IL} < 0.4, V_{IH} > 2.4$) or high level clock ($V_{IL} < 0.2, V_{IH} = Vcc^{+.3}_{-.2}$).

Read/Write (R/W)

The R/W signal is supplied by the microprocessor array and is used to control the transfer of data to and from the microprocessor array and the 6530. A high on the R/W pin allows the processor to read (with proper addressing) the data supplied by the 6530. A low on the R/W pin allows a write (with proper addressing) to the 6530.

Interrupt Request ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an interrupt pin from the interval timer. This same pin, if not used as an interrupt, can be used as a peripheral I/O pin (PB7). When used as an interrupt, the pin should be set up as an input by the data direction register. The pin will be normally high with a low indicating an interrupt from the 6530. An external pull-up device is not required; however, if collector-OR'd with other devices, the internal pullup may be omitted with a mask option.

Data Bus (D0-D7)

The 6530 has eight bi-directional data pins (D0-D7). These pins connect to the system's data lines and allow transfer of data to and from the microprocessor array. The output buffers remain in the off state except when a Read operation occurs.

Peripheral Data Ports

The 6530 has 16 pins available for peripheral I/O operations. Each pin is individually software programmable to act as either an input or an output. The 16 pins are divided into 2 8-bit ports, PA0-PA7 and PB0-PB7. PB5, PB6 and PB7 also have other uses which are discussed in later sections. The pins are set up as an input by writing a "0" into the corresponding bit of the data direction register. A "1" into the data direction register will cause its corresponding bit to be an output. When in the input mode, the peripheral output buffers are in the "1" state and a pull-up device acts as less than one TTL load to the periphera data lines. On a Read operation, the microprocessor unit reads the peripheral pin. When the peripheral device gets information from the 6530 it receives data stored in the data register. The microprocessor will read correct information if the peripheral lines are greater than 2.0 volts for a "1" and less than 0.8 volts for a "0" as the peripheral pins are all TTL compatible. Pins PA0 and PB0 are also capable of sourcing 3 ma at 1.5v, thus making them capable of Darlington drive.

Address Lines (A0-A9)

There are 10 address pins. In addition to these 10, there is the ROM SELECT pin. The above pins, A0-A9 and ROM SELECT, are always used as addressing pins. There are 2 additional pins which are mask programmable and can be used either individually or together as CHIP SELECTS. They are pins PB5 and PB6. When used as peripheral data pins they cannot be used as chip selects.

ADDRESSING

Addressing of the 6530 offers many variations to the user for greater flexibility. The user may configure his system with RAM in lower memory, ROM in higher memory, and I/O registers with interval timers between the extremes. There are 10 address lines (A0-A9). In addition, there is the possibility of 3 additional address lines to be used as chip-selects and to distinguish between ROM, RAM, I/O and interval timer. Two of the additional lines are chip-selects 1 and 2 (CS1 and CS2). The chip-select pins can also be PB5 and PB6. Whether the pins are used as chip-selects or peripheral I/O pins is a mask option and must be specified when ordering the part. Both pins act independently of each other in that either or both pins may be designated as a chip-select. The third additional address line is RS0. The 6502 and 6530 in a 2-chip system would use RS0 to distinguish between ROM and non-ROM sections of the 6530. With the addressing pins available, a total of 7K contiguous ROM may be addressed with no external decode. Below is an example of a 1-chip and a 7-chip 6530 Addressing Scheme.

One-Chip Addressing

Figure 6 illustrates a 1-chip system decode for the 6530.

Seven-Chip Addressing

In the 7-chip system the objective would be to have 7K of contiguous ROM, with RAM in low order memory. The 7K of ROM could be placed between addresses 65,535 and 1024. For this case, assume A13, A14 and A15 are all 1 when addressing ROM, and 0 when addressing RAM or I/O. This would place the 7K ROM between Addresses 65,535 and 58,367. The 2 pins designated as chip-select or I/O would be masked programmed as chip-select pins. Pin RS0 would be connected to address line A10. Pins CS1 and CS2 would be connected to address lines A11 and A12 respectively. See Figure 7.

The two examples shown would allow addressing of the ROM and RAM; however, once the I/O or timer has been addressed, further decoding is necessary to select which of the I/O registers are desired, as well as the coding of the interval timer.

I/O Register — Timer Addressing

Figure 8 illustrates the address decoding for the internal elements and timer programming. Address lines A2 distinguishes I/O registers from the timer. When A2 is high and I/O timer select is high, the I/O registers are addressed. Once the I/O registers are addressed, address lines A1 and A0 decode the desired register.

When the timer is selected A1 and A0 decode the divide by matrix. This decoding is defined in Figure 8. In addition, Address A3 is used to enable the interrupt flag to PB7.

When the timer has counted down to 0 0 0 0 0 0 0 0 on the next count time an interrupt will occur and the counter will read 1 1 1 1 1 1 1 1. After interrupt, the timer register decrements at a divide by "1" rate of the system clock. If after interrupt, the timer is read and a value of 1 1 1 0 0 1 0 0 is read, the time since interrupt is 28T. The value read is in two's complement.

Value read = 1 1 1 0 0 1 0 0
Complement = 0 0 0 1 1 0 1 1
ADD 1 = 0 0 0 1 1 1 0 0 = 28.

Thus, to arrive at the **total** elapsed time, merely do a two's complement add to the original time written into the timer. Again, assume time written as 0 0 1 1 0 1 0 0 (=52). With a divided by 8, total time to interrupt is (52 x 8) + 1 = 417T. Total elapsed time would be 416T + 28T = 444T, assuming the value read after interrupt was 1 1 1 0 0 1 0 0.

After the interrupt, whenever the timer is written or read the interrupt is reset. However, the reading of the timer at the same time the interrupt occurs will not reset the interrupt flag. When the interrupt flag is read on DB7 all other DB outputs (DB0 thru DB6) go to "0". Figure 5 illustrates an example of interrupt.

When reading the timer after an interrupt, A3 should be low so as to disable the $\overline{IRQ}$ pin. This is done so as to avoid future interrupts until after another Write timer operation.

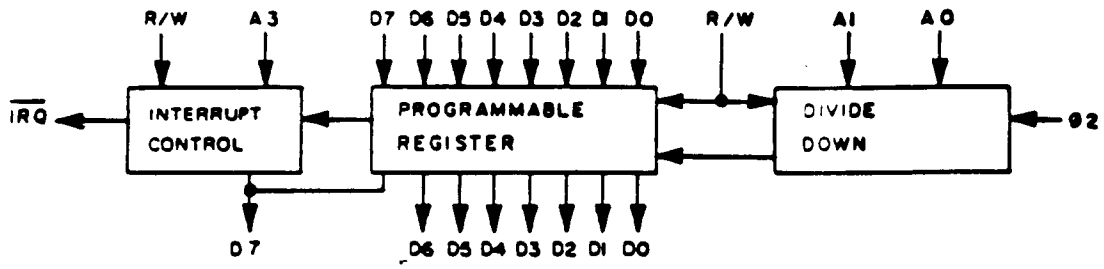
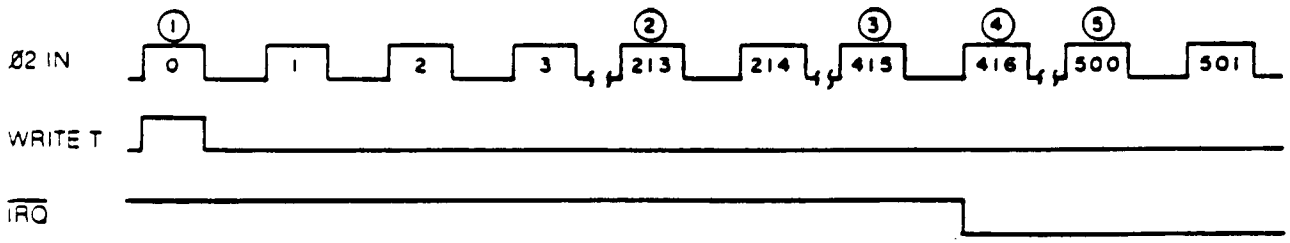


Figure 4. Basic Elements of Interval Timer



1. Data written into interval timer is 0 0 1 1 0 1 0 0 = 52_{10}
2. Data in interval timer is 0 0 0 1 1 0 0 1 = 25_{10}
   $52 - \frac{213}{8} - 1 = 52\text{-}26\text{-}1 = 25$
3. Data in interval timer is 0 0 0 0 0 0 0 0 = 0_{10}
   $52 - \frac{415}{8} - 1 = 52\text{-}51\text{-}1 = 0$
4. Interrupt has occurred at $Ø_2$ pulse #416
   Data in interval timer = 1 1 1 1 1 1 1 1
5. Data in interval timer is 1 0 1 0 1 1 0 0
   two's complement is 0 1 0 1 0 1 0 0 = 84_{10}
   $84 \div (52 \times 8) = 500_{10}$

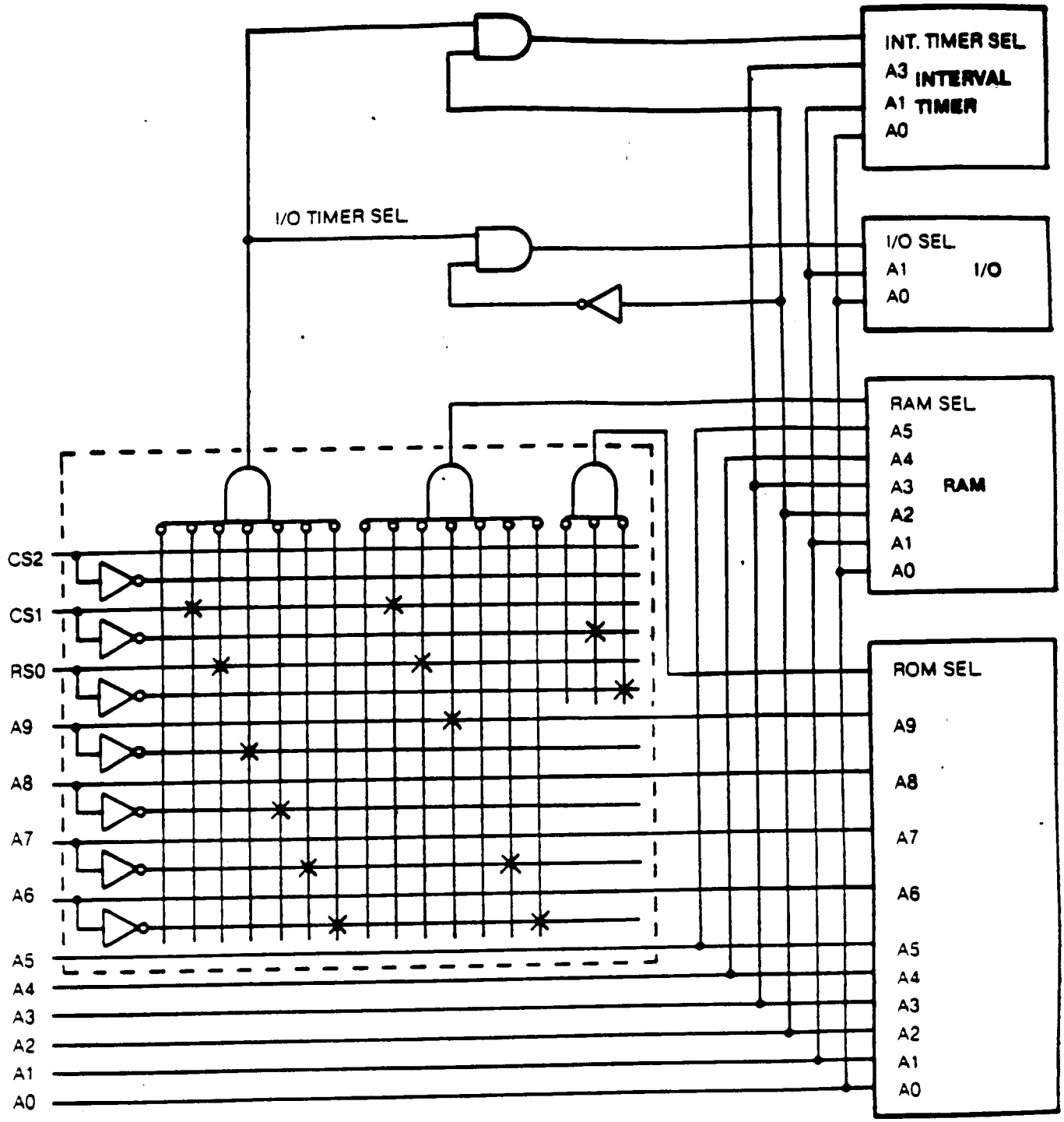
Figure 5

The addressing of the ROM select, RAM select and I/O Timer select lines would be as follows:

		CS2 A12	CS1 A11	RS0 A10	A9	A8	A7	A6
6530 #1.	ROM SELECT	0	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	0
	I/O TIMER	0	0	0	1	0	0	0
6530 #2.	ROM SELECT	0	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	0	1
	I/O TIMER	0	0	0	1	0	0	1
6530 #3.	ROM SELECT	0	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	0
	I/O TIMER	0	0	0	1	0	1	0
6530 #4.	ROM SELECT	1	0	0	X	X	X	X
	RAM SELECT	0	0	0	0	0	1	1
	I/O TIMER	0	0	0	1	0	1	1
6530 #5.	ROM SELECT	1	0	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	0
	I/O TIMER	0	0	0	1	1	0	0
6530 #6.	ROM SELECT	1	1	0	X	X	X	X
	RAM SELECT	0	0	0	0	1	0	1
	I/O TIMER	0	0	0	1	1	0	1
6530 #7.	ROM SELECT	1	1	1	X	X	X	X
	RAM SELECT	0	0	0	0	1	1	0
	I/O TIMER	0	0	0	1	1	1	0

*RAM select for 6530 #5 would read = $\overline{A12} \bullet \overline{A11} \bullet \overline{A10} \bullet \overline{A9} \bullet A8 \bullet \overline{A7} \bullet \overline{A6}$

Figure 7. 6530 Seven Chip Addressing Scheme



A. X indicates mask programming
   i.e. ROM select=$\overline{CS1} \bullet RS0$
   RAM select=$\overline{CS1} \bullet \overline{RS0} \bullet \overline{A9} \bullet A7 \bullet A6$
   I/O TIMER SELECT=$\overline{CS1} \bullet \overline{RS0} \bullet A9 \bullet A8 \bullet A7 \bullet A6$
B. Notice that A8 is a don't care for RAM select
C. CS2 can be used as PB5 in this example.

Figure 6. 6530 One Chip Address Encoding Diagram

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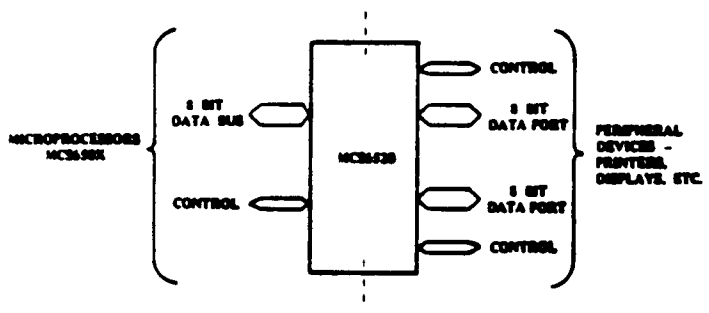
MCS6520 PERIPHERAL ADAPTER

DESCRIPTION

The MCS6520 Peripheral Adapter is designed to solve a broad range of peripheral control problems in the implementation of microcomputer systems. This device allows a very effective trade-off between software and hardware by providing significant capability and flexibility in a low cost chip. When coupled with the power and speed of the MCS6500 family of microprocessors, the MCS6520 allows implementation of very complex systems at a minimum overall cost.

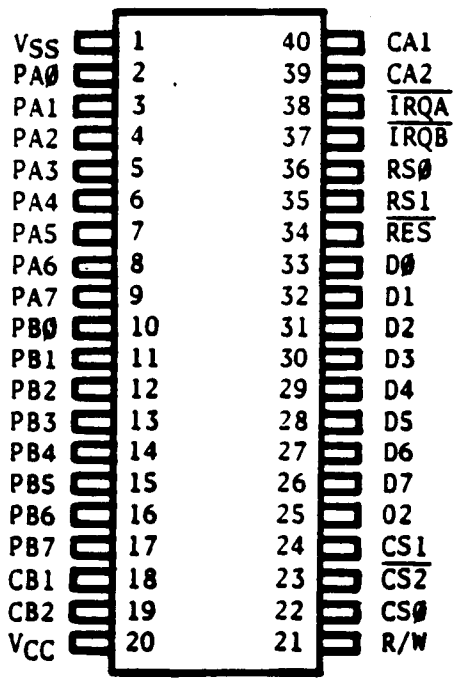
Control of peripheral devices is handled primarily through two 8-bit bi-directional ports. Each of these lines can be programmed to act as either an input or an output. In addition, four peripheral control/interrupt input lines are provided. These lines can be used to interrupt the processor or for "hand-shaking" data between the processor and a peripheral device.

- High performance replacement for Motorola/AMI/MOSTEK/Hitachi peripheral adapter.
- N channel, depletion load technology, single +5V supply.
- Completely Static and TTL compatible.
- CMOS compatible peripheral control lines.
- Fully automatic "hand-shake" allows very positive control of data transfers between processor and peripheral devices.



Basic MCS6520 Interface Diagram

MCS6520



SUMMARY OF MCS6520 OPERATION

See MOS TECHNOLOGY Microcomputer Hardware Manual for detailed description of MCS6520 operation.

CA1/CB1 CONTROL

CRA (CRB) Bit 1	CRA (CRB) Bit 0	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Outputs
0	0	negative	Disable--remain high
0	1	negative	Enable--goes low when bit 7 in CRA (CRB) is set by active transition of signal on CA1 (CB1)
1	0	positive	Disable--remain high
1	1	positive	Enable--as explained above

*Note: Bit 7 of CRA (CRB) will be set to a logic 1 by an active transition of the CA1 (CB1) signal. This is independent of the state of Bit 0 in CRA (CRB).

CA2/CB2 INPUT MODES

CRA (CRB) Bit 5	CRA (CRB) Bit 4	CRA (CRB) Bit 3	Active Transition of Input Signal*	IRQA (IRQB) Interrupt Output
0	0	0	negative	Disable--remains high
0	0	1	negative	Enable--goes low when bit 6 in CRA (CRB) is set by active transition of signal on CA2 (CB2)
0	1	0	positive	Disable--remains high
0	1	1	positive	Enable--as explained above

*Note: Bit 6 of CRA (CRB) will be set to a logic 1 by an active transition of the CA2 (CB2) signal. This is independent of the state of Bit 3 in CRA (CRB).

CA2 OUTPUT MODES

CRA Bit 5	CRA Bit 4	CRA Bit 3	Mode	Description
1	0	0	"Handshake" on Read	CA2 is set high on an active transition of the CA1 interrupt input signal and set low by a microprocessor "Read A Data" operation. This allows positive control of data transfers from the peripheral device to the microprocessor.
1	0	1	Pulse Output	CA2 goes low for one cycle after a "Read A Data" operation. This pulse can be used to signal the peripheral device that data was taken.
1	1	0	Manual Output	CA2 set low
1	1	1	Manual Output	CA2 set high

CB2 OUTPUT MODES

CRB Bit 5	CRB Bit 4	CRB Bit 3	Mode	Description
1	0	0	"Handshake" on Write	CB2 is set low on microprocessor "Write B Data" operation and is set high by an active transition of the CB1 interrupt input signal. This allows positive control of data transfers from the microprocessor to the peripheral device.
1	0	1	Pulse Output	CB2 goes low for one cycle after a microprocessor "Write B Data" operation. This can be used to signal the peripheral device that data is available.
1	1	0	Manual Output	CB2 set low
1	1	1	Manual Output	CB2 set high

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.3 to +7.0	V_{dc}
Input Voltage	V_{in}	-0.3 to +7.0	V_{dc}
Operating Temperature Range	T_A	0 to +70	^oC
Storage Temperature Range	T_{stg}	-55 to +150	^oC

This device contains circuitry to protect the inputs against damage due to high static voltages, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this circuit.

STATIC D.C. CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage (Normal Operating Levels)		V_{IH}	+2.0	-	V_{CC}	Vdc
Input Low Voltage (Normal Operating Levels)		V_{IL}	-0.3	-	+.8	Vdc
Input Threshold Voltage		V_{IT}	0.8	-	2.0	Vdc
Input Leakage Current		I_{IN}				uAdc
V_{in} = 0 to 5.0 Vdc	R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, ϕ2		-	±1.0	±2.5	
Three-State (Off State Input Current		I_{TSI}				
(V_{in} = 0.4 to 2.4 Vdc, V_{CC} = max)	D0-D7, PB0-PB7, CB2		-	±2.0	±10	uAdc
Input High Current		I_{IH}				
(V_{IH} = 2.4 Vdc)	PA0-PA7, CA2		-100	-250	-	uAdc
Input Low Current		I_{IL}				
(V_{IL} = 0.4 Vdc)	PA0-PA7, CA2		-	-1.0	-1.6	mAdc
Output High Voltage		V_{OH}				
(V_{CC} = min, I_{Load} = -100 uAdc)			2.4	-	-	Vdc
Output Low Voltage		V_{OL}				
(V_{CC} = min, I_{Load} = 1.6 mAdc)			-	-	+0.4	Vdc
Output High Current (Sourcing)		I_{OH}				
(V_{OH} = 2.4 Vdc)			-100	-1000	-	uAdc
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base)	PB0-PB7, CB2		-1.0	-2.5	-	mAdc
Output Low Current (Sinking)		I_{OL}				
(V_{OL} = 0.4 Vdc)			1.6	-	-	mAdc
Output Leakage Current (Off State)	$\overline{IRQA}$, $\overline{IRQB}$	I_{off}	-	1.0	10	uAdc
Power Dissipation		P_D	-	200	500	mW
Input Capacitance		C_{in}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7, PA0-PA7, PB0-PB7, CA2, CB2		-	-	10	
	R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, CS2,		-	-	7.0	
	CA1, CB1, ϕ2		-	-	20	
Output Capacitance		C_{out}				
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)			-	-	10	pF

NOTE: Negative sign indicates outward current flow, positive indicates inward flow.

FIGURE 1 – READ TIMING CHARACTERISTICS

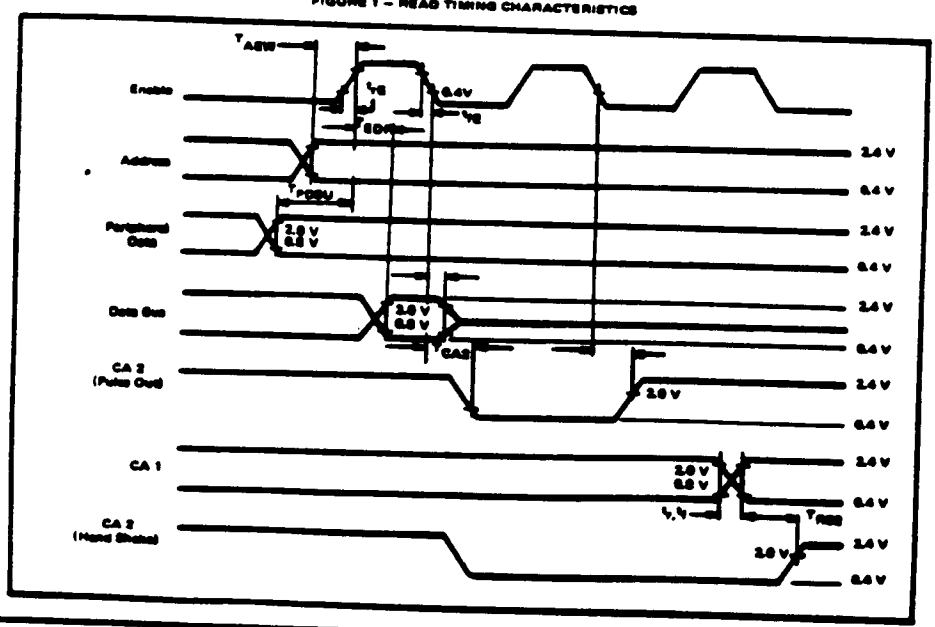
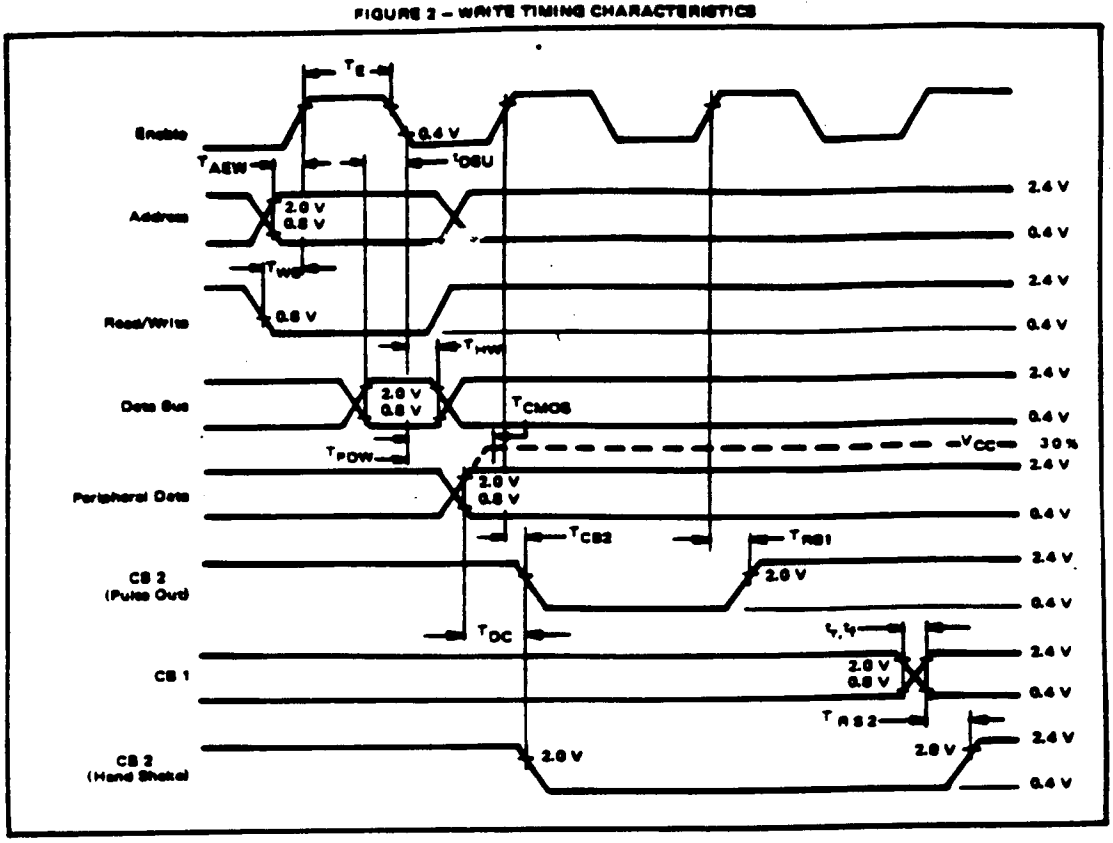


FIGURE 2 – WRITE TIMING CHARACTERISTICS



A.C. CHARACTERISTICS

Read Timing Characteristics (Figure 1, Loading 130 pF and one TTL load)

Characteristics	Symbol	Min	Typ	Max	Unit
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	-	-	ns
Delay Time, Enable positive transition to Data valid on bus	T_{EDR}	-	-	395	ns
Peripheral Data Setup Time	T_{PDSU}	300	-	-	ns
Data Bus Hold Time	T_{HR}	10	-	-	ns
Delay Time, Enable negative transition to CA2 negative transition	T_{CA2}	-	-	1.0	us
Delay Time, Enable negative transition to CA2 positive transition	T_{RS1}	-	-	1.0	us
Rise and Fall Time for CA1 and CA2 input signals	t_r, t_f	-	-	1.0	us
Delay Time from CA1 active transition to CA2 positive transition	T_{RS2}	-	-	2.0	us
Rise and Fall Time for Enable input	t_{rE}, t_{fE}	-	-	25	us

Write Timing Characteristics (Figure 2)

Characteristics	Symbol	Min	Typ	Max	Unit
Enable Pulse Width	T_E	0.470	-	25	us
Delay Time, Address valid to Enable positive transition	T_{AEW}	180	-	-	ns
Delay Time, Data valid to Enable negative transition	T_{DSU}	300	-	-	ns
Delay Time, Read/Write negative transition to Enable positive transition	T_{WE}	130	-	-	ns
Data Bus Hold Time	T_{HW}	10	-	-	ns
Delay Time, Enable negative transition to Peripheral Data valid	T_{PDW}	-	-	1.0	us
Delay Time, Enable negative transition to Peripheral Data Valid, CMOS (V_{CC} - 30%) PA0-PA7, CA2	T_{CMOS}	-	-	2.0	us
Delay Time, Enable positive transition to CB2 negative transition	T_{CB2}	-	-	1.0	us
Delay Time, Peripheral Data valid to CB2 negative transition	T_{DC}	0	-	1.5	us
Delay Time, Enable positive transition to CB2 positive transition	T_{RS1}	-	-	1.0	us
Rise and Fall Time for CB1 and CB2 input signals	t_r, t_f	-	-	1.0	us
Delay Time, CB1 active transition to CB2 positive transition	T_{RS2}	-	-	2.0	us