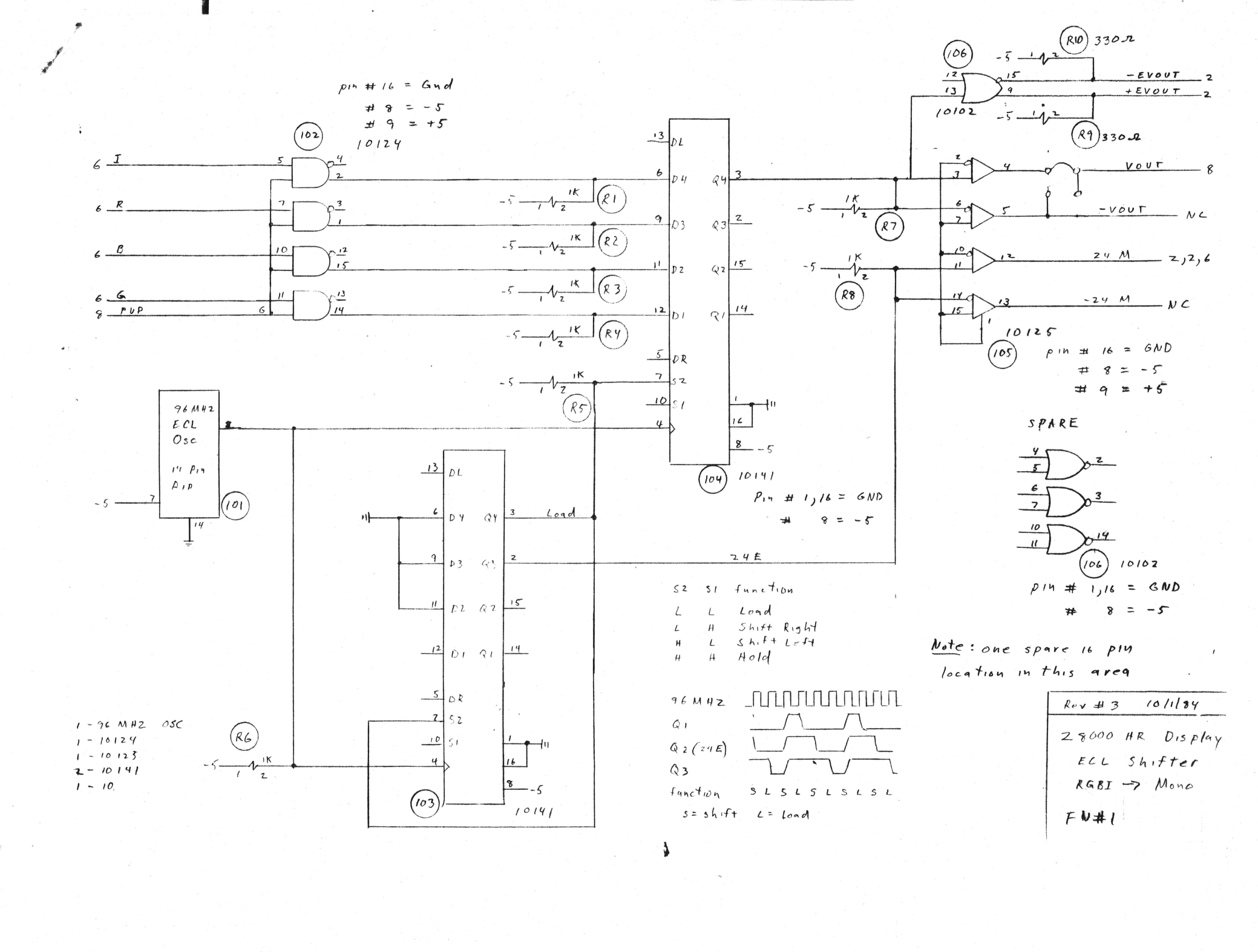
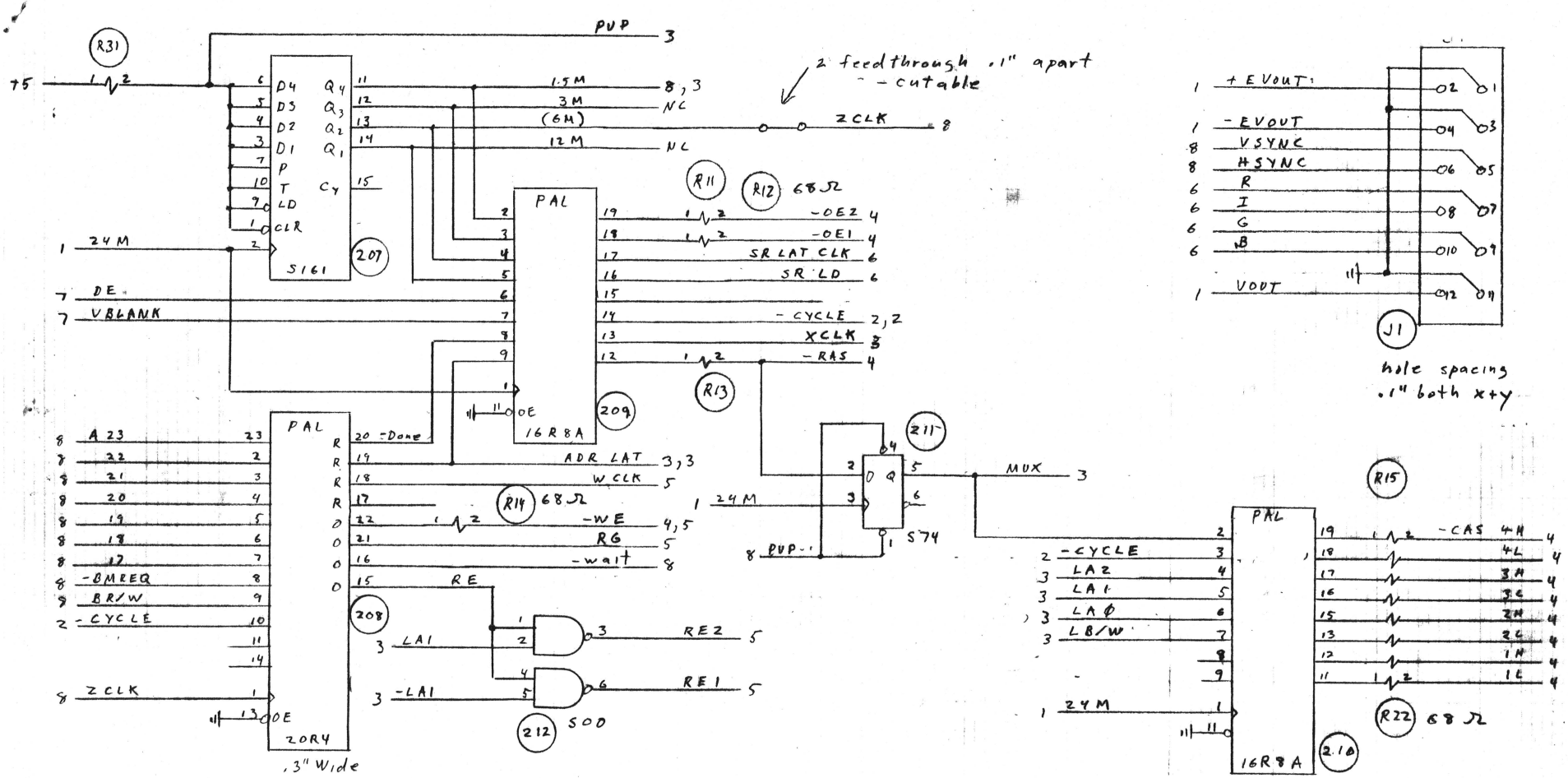

pin # 16 = Gnd
# 8 = -5
# 9 = +5
10124
102
6 I
6 R
6 B
6 G
8 PUP
R1
R2
R3
R4
R5
R6
R7
R8
R9 330Ω
R10 330Ω
1K
-5
104
10141
DL
D4
D3
D2
D1
DR
S2
S1
Q4
Q3
Q2
Q1
Load
24E
Pin # 1,16 = GND
# 8 = -5
96 MHz
ECL
Osc
14 Pin
DIP
101
103
106
10102
-EVOUT
+EVOUT
VOUT
-VOUT
24 M
-24 M
NC
2,3,6
2
8
10125
105
pin # 16 = GND
# 8 = -5
# 9 = +5
SPARE
S2 S1 function
L L Load
L H Shift Right
H L Shift Left
H H Hold
96 MHz
Q1
Q2 (24E)
Q3
function S L S L S L S L S L
S = shift L = Load
Note: one spare 16 pin location in this area
1 - 96 MHz OSC
1 - 10124
1 - 10123
2 - 10141
1 - 10
Rev # 3 10/1/84
28000 HR Display
ECL Shifter
RGBI → Mono
FN#1

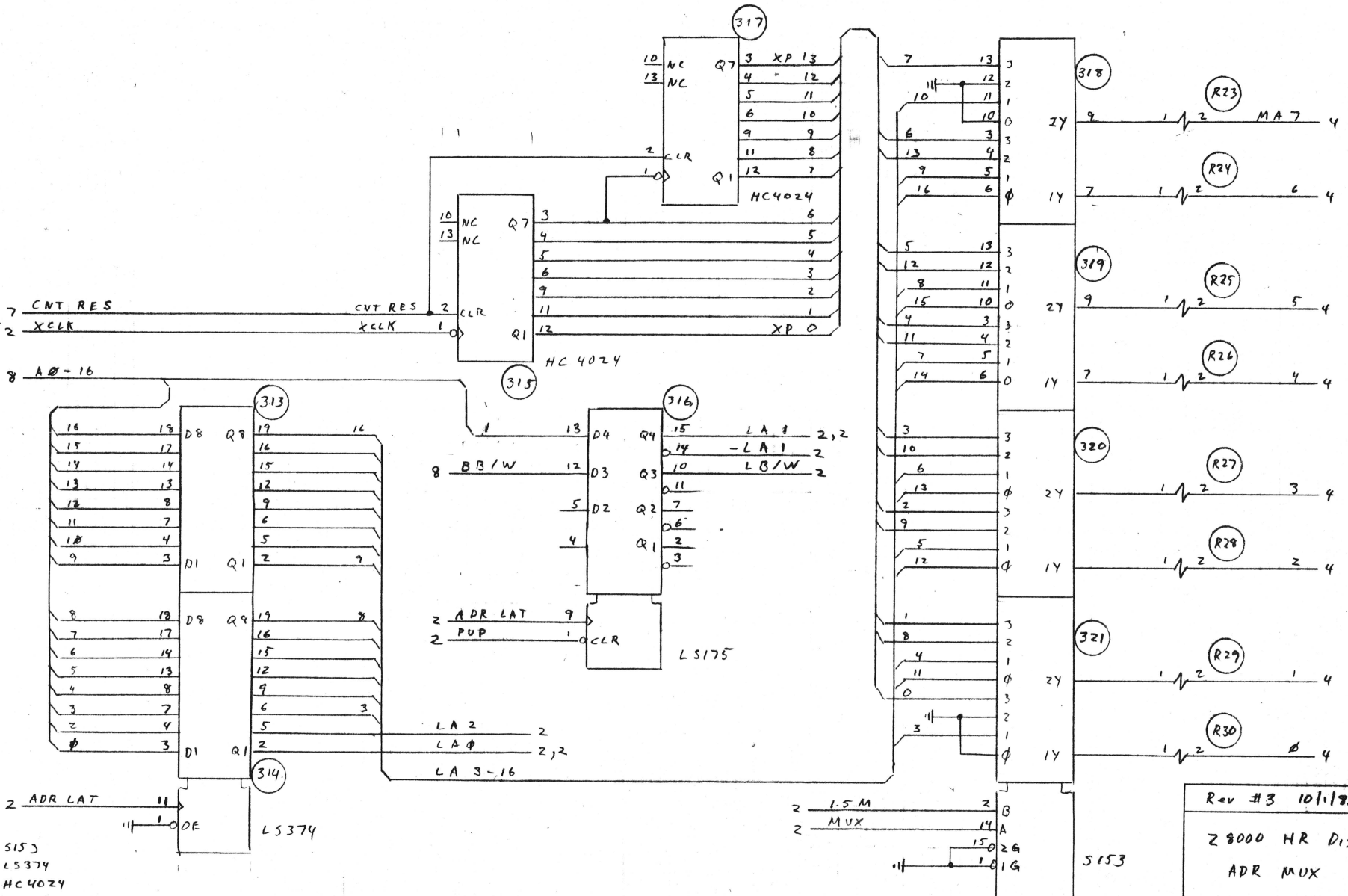


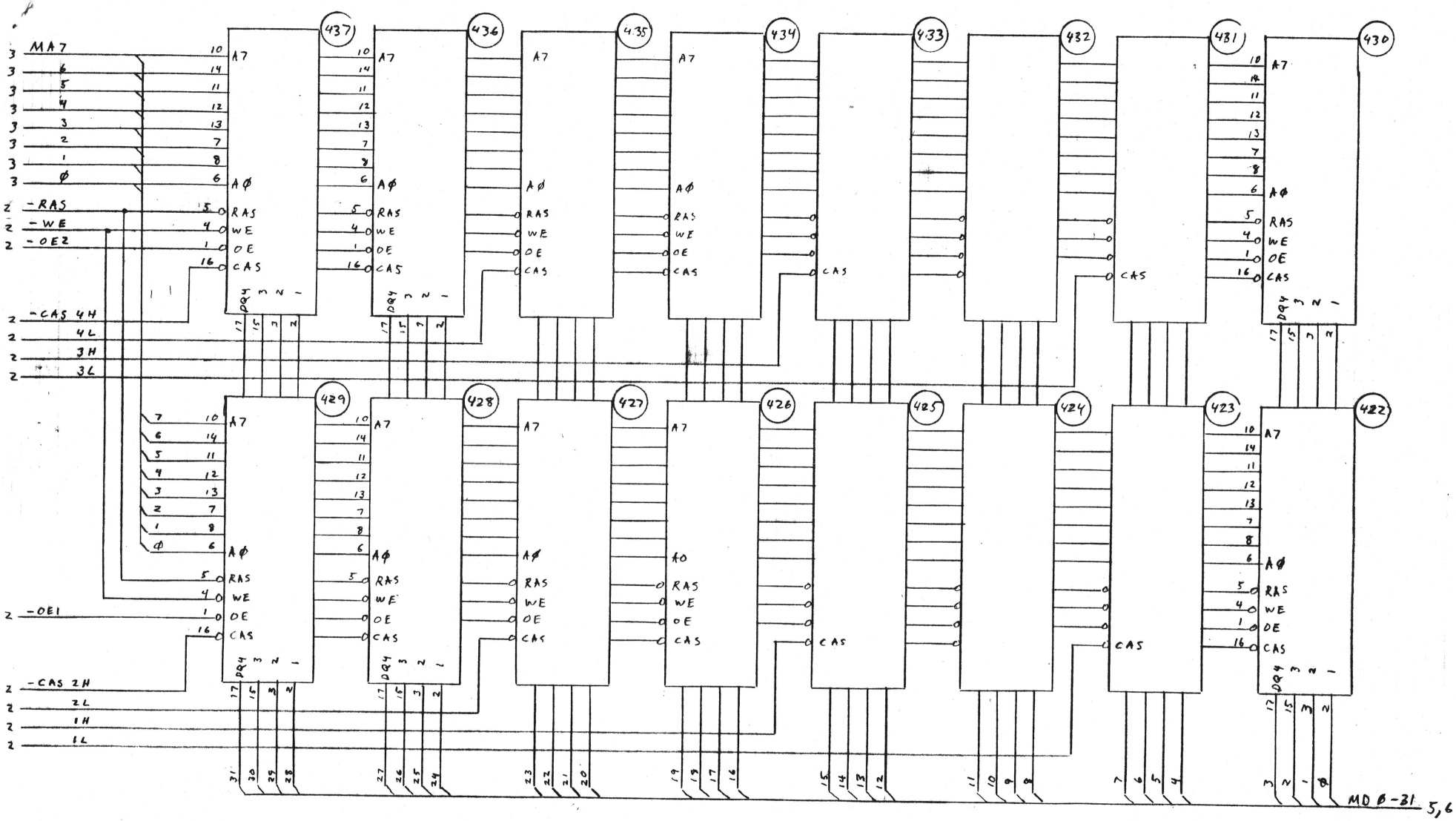

1 - S161
1 - 16R8A
1 - 20R4
1 - S74
.5 - S00
1 - 82S100

5.5 chips

212

| Rev #3 10/1/84 |
| --- |
| Z8000 HR Display Memory Control |
| FN# 2 |


317
318
319
320
321
315
316
313
314
R23
R24
R25
R26
R27
R28
R29
R30
HC4024
HC 4024
LS175
LS374
S153
CNT RES
XCLK
A0-16
BB/W
ADR LAT
PUP
1.5M
MUX
LA 1
-LA 1
LB/W
LA 2
LA 0
LA 3-16
XP 13
XP 0
MA 7
4 - S153
2 - LS374
2 - HC4024
1 - LS175
9 chips
Rev #3 10/1/84
Z 8000 HR Display
ADR MUX
FN#3
321




Note : 4416 DRAM's
pin # 18 = GND
9 = +5

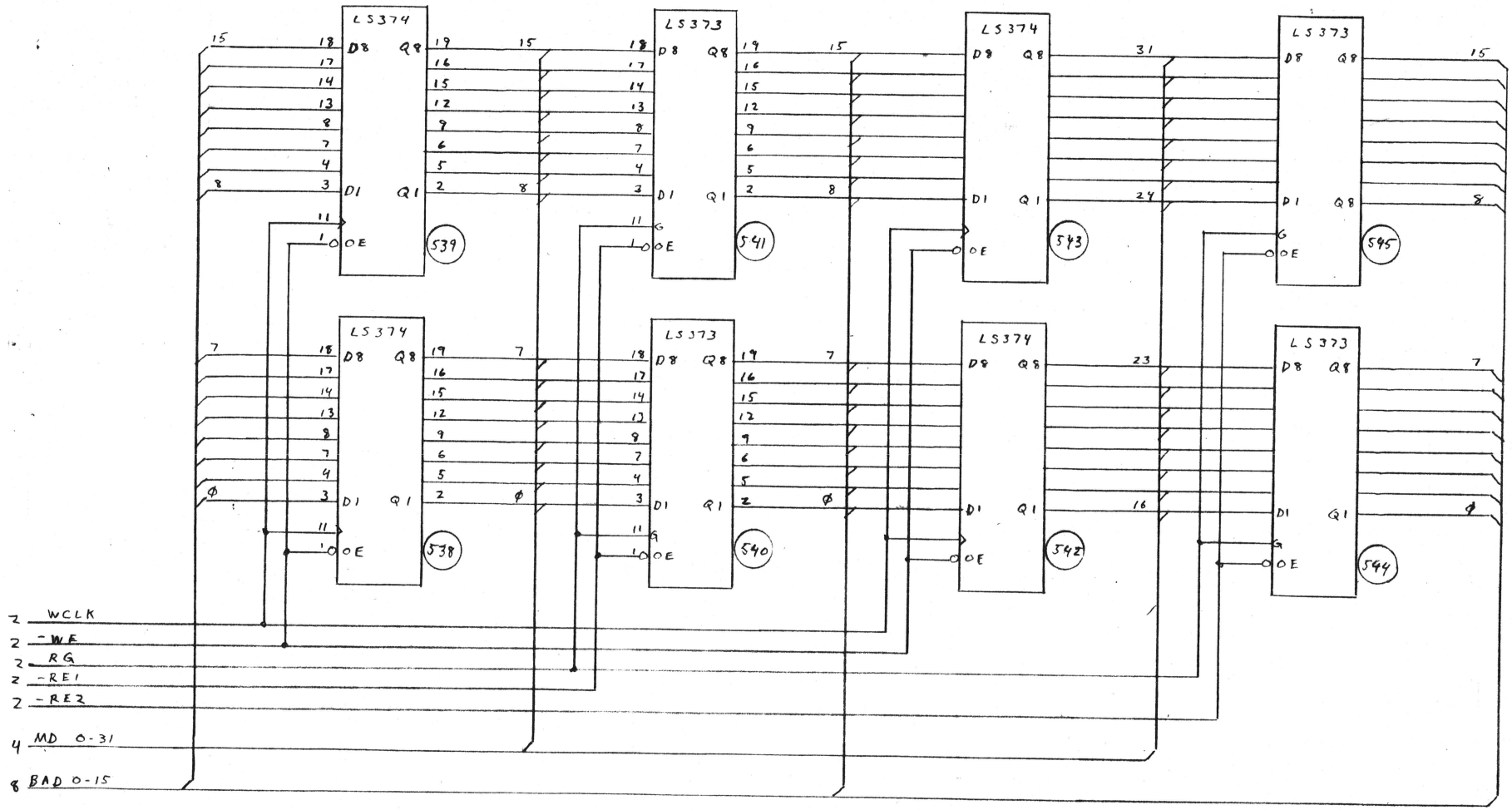
one .22 uf per chip

Rev #3 10/1/84

Z8000 HR Display Memory Array

FN # 4

437



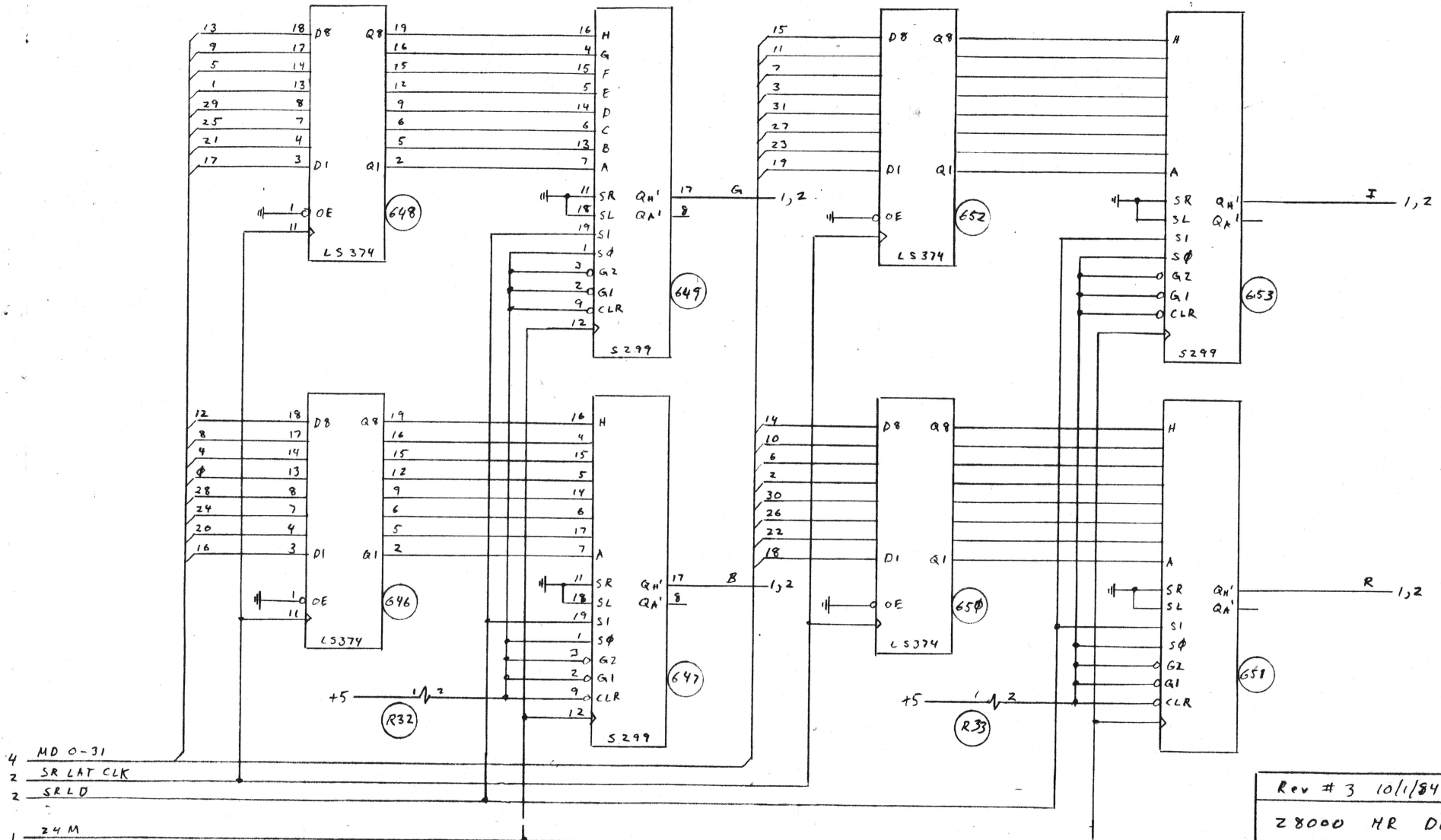

4 - LS 373
4 - LS 374

545

Rev #3 10/1/84

Z8000 HR Display
Data Latch Array

FN#5

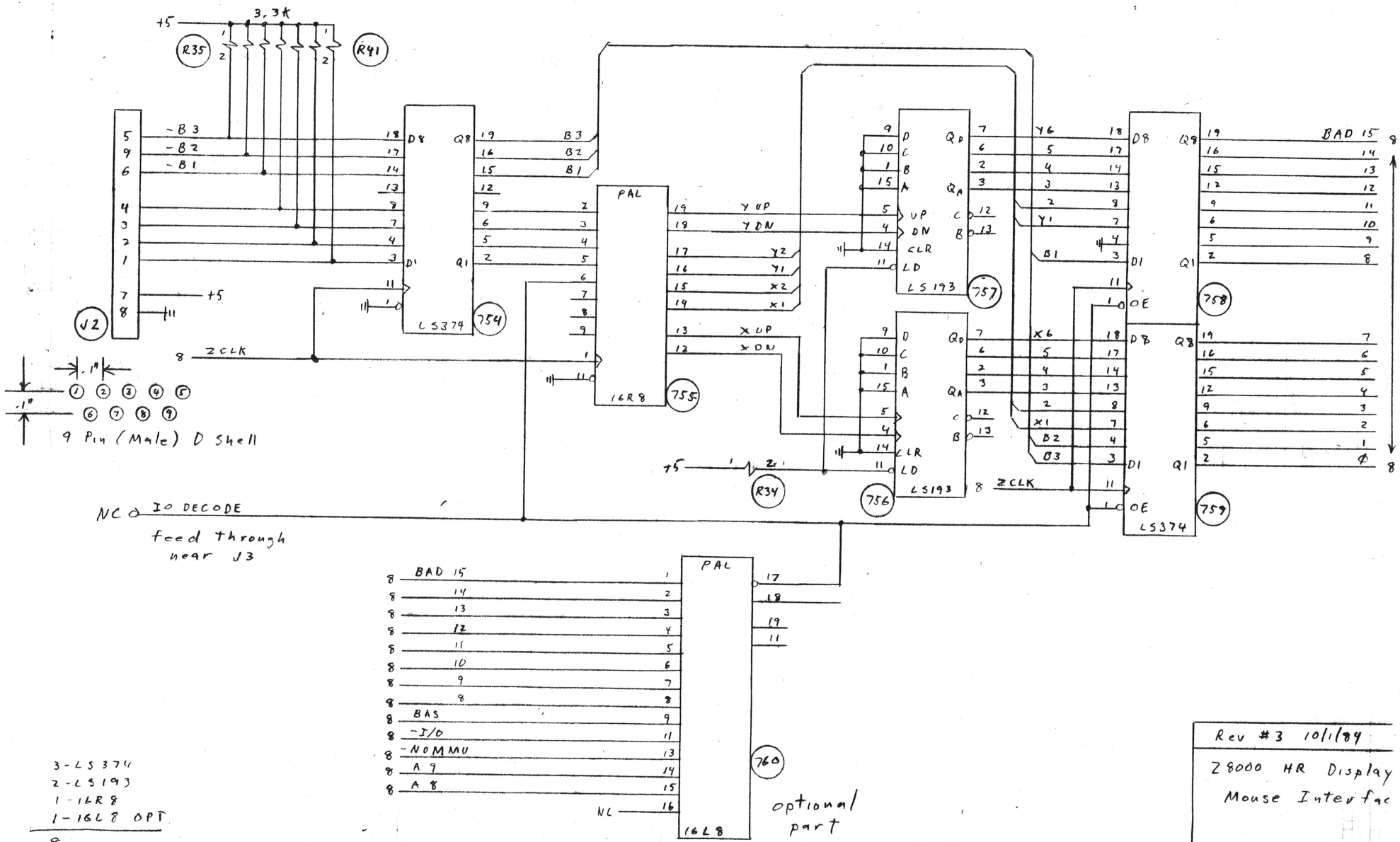



Rev # 3 10/1/84

Z8000 HR Displ Shift Register Array

FN# 6

653




3-LS374
2-LS193
1-16R8
1-16L8 OPT

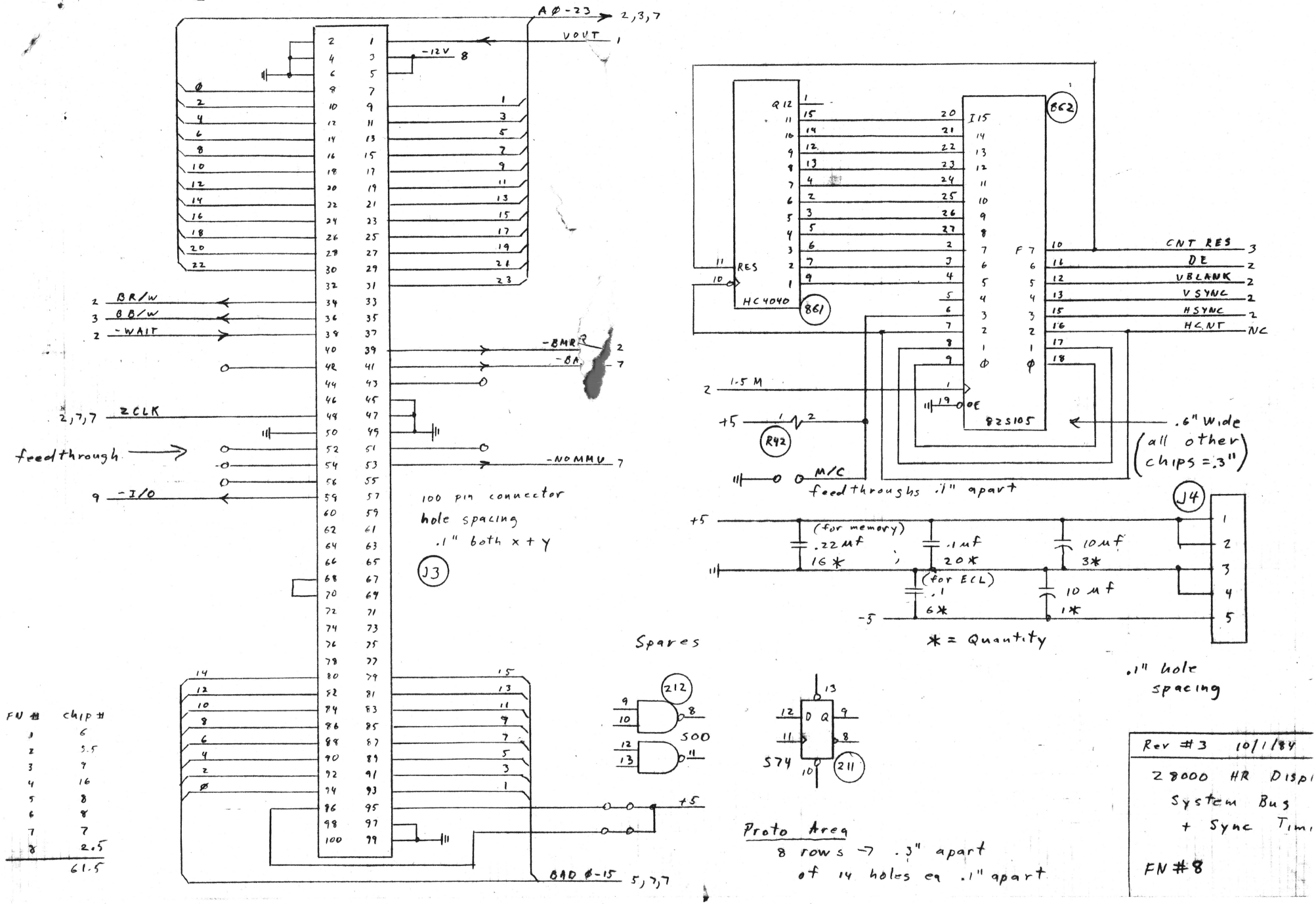
8

760

Rev #3 10/1/84

Z8000 HR Display
Mouse Interface

FN#7




| FN # | chip # |
|---|---|
| 1 | 6 |
| 2 | 5.5 |
| 3 | 9 |
| 4 | 16 |
| 5 | 8 |
| 6 | 8 |
| 7 | 7 |
| 8 | 2.5 |
| | 61.5 |

| Rev #3 | 10/1/84 |
|---|---|
| 28000 HR Displ | |
| System Bus | |
| + Sync Timi | |
| FN #8 | |